EMPIR Call 2014 – Industry and Research Potential

Selected Research Topic number: **SRT-i21**
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Title: Metrology for manufacturing 3D stacked integrated circuits

Abstract

The European Electronic Leaders Group roadmap [1] identified three-dimensional stacked integrated circuits (3D-SICs) as the next big innovation in electronics. 3D-SICs are expected to achieve shorter wirelength, smaller critical path delay and less power consumption with increased functionality by integrating logic, memory, sensor and actuators in compact systems. However, for high-volume production, several challenges remain, some of them related to the associated metrology and inspection for the 3D integration where various key technologies are required: Through Silicon Vias (TSV) [2], wafer/chip thinning and wafer/chip bonding. Traceable metrological infrastructure and facilities for 3D thermal and electrical materials characterisation, defects inspection for high-aspect ratio TSV and wafer/chip bonding and thinning need to be developed.

Keywords

3D technology, 3D heterogeneous integration, 3D-SICs, TSVs, wafer stacking, metrology, nanoelectronics, nanoscale characterisation

Background to the Metrological Challenges

Performance requirements in the electronics industry can no longer be met by downscaling Si-based complementary metal–oxide–semiconductor (CMOS) devices. The semiconductor industry is looking for new solutions: miniaturisation or “More Moore”; diversification and integration or “More-than-Moore”, and “Beyond CMOS” i.e. graphene, spintronic, molecular electronic etc. For the More-than-Moore approach new 3D architectures are being developed and introduced as 3D stacked integrated circuits (3D-SICs). In these, the electronic components are stacked by superimposing dies and/or wafers, and 3D short electrical connections are established between the components directly through the various layers. Copper damascene Through Silicon Vias (TSV) are used as 3D interconnects through a stack of chip-bonded semiconductor wafers and dies to produce optimised multilevel chips [3, 4]. When proven feasible and economic for volume manufacturing, this will provide a path toward integrating diverse CMOS technologies e.g. logic devices, memories, imagers and MEMS structures. The key technology bricks that are preventing their cost-effective implementation in production have been identified [5]: TSV interconnects realisation (filling quality, low resistivity, isolation, delay and reliability), bonding quality (interface defects, adhesion strength); wafer alignment accuracy and wafer/die level thinning (thickness control, roughness, topography, surface defects, strain-stress relaxation). Consequently, relevant metrology and measurement techniques need to be developed to understand and control such production line issues.

TSV technology will be crucial as it can be integrated in industrial production, it has high-density interconnect capabilities and it can be miniaturised at the chip and wafer level. The smallest TSVs are around a few µm and this is expected to reach sub-micron dimensions in a few years. The challenges that must be addressed through 3D characterisation, metrology (non-destructive wafer measurements) and defectivity include: sidewall smoothness, isolation uniformity of the TSV sidewall, conformity of copper seed and diffusion layers at the sidewall and void-free copper electroplating. Imaging of a representative set of TSVs will be needed, as will representative sampling with automatic pattern recognition. In addition, nanometric resolution will need to be developed to address seed and diffusion-barrier metrology and characterisation.

Copper has significant advantages; however TSVs with reduced dimensions show an increase in resistivity and operational temperature. Power dissipation may even lead to the replacement of copper with another metal. Direct nanoscale conductivity measurements need to be performed. NB standard resistive electrical test structures used to measure the linewidth of conducting tracks assume a homogeneous layer of conducting material, which is not the case for copper damascene interconnects, as barrier layers are used.

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It will also be important to investigate accurate methods for controlling and characterising the bonding quality at the wafers/die level: initial curvature, surface roughness, flatness, topography and contamination before bonding; interface defectivity and adhesion after bonding; and local stress and thermal dissipation at the interface. Another challenge is wafer thinning and chemical mechanical planarisation (CMP) particularly in the presence of high topography as Cu pillar bumps or Cu nails at TSV reveal step. This can cause the wafer/die to bow locally leading to additional topography, wafer deformation and local thickness variations. Measuring the residual silicon thickness above the TSVs is more complicated if the back surface of the wafer is rough. In addition, the thinning process itself can cause crystalline defects, surface contamination and stress relaxation, which need to be well characterised to prevent any failure of 3D-SIC devices.

Current state-of-the-art measurement techniques lack traceability, accuracy and quantification. Therefore, 3D characterisation, metrology and inspection with micrometric to nanometric resolution and large-field analysis to inspect and measure groups of vias are required. This will enable control of key parameters such as copper voids at vias filling, seed and diffusion barrier conformity at the TSV sidewall.

Objectives

Proposers should address the objectives stated below, which are based on the PRT submissions. Proposers may identify amendments to the objectives or choose to address a subset of them in order to maximise the overall impact, or address budgetary or scientific / technical constraints, but the reasons for this should be clearly stated in the proposal.

The JRP shall focus on the development of metrology for manufacturing 3D stacked integrated circuits.

The specific objectives are

1. To develop reliable 3D characterisation techniques, protocols and standards to accurately measure (at micron and submicron resolution) dimensional and structural properties of high aspect ratio (>10) Through Silicon Vias (TSV) interconnects before and after Cu filling. Properties that should be considered include sidewall roughness, via shape, seed- and barrier-layer thickness, sidewall layer conformity, void detection and characterisation, grain size and grain boundary character, distribution of the copper grains, crystalline structure, dislocations, and the stress around the TSV. For 3D-SICs with high density TSV interconnects, non-destructive wafer measurements and statistical data collection should be developed in order to enable the implementation of the measurement techniques in a production environment.
2. To develop methods to measure the electrical and thermal transport properties of nanostructured copper TSV interconnects in order to establish traceable measurements of electrical conductivity and temperature change in copper as a function of the current density (ideally without using test structures). The accuracy of these new methods should be significantly better than the current state of the art. The developed techniques should assist in identifying the various thermal scattering mechanisms in nanostructured copper grains.
3. To develop metrology tools, protocols and standards for high lateral and z resolution (submicron for x-y, nm for z) non-destructive wafer to wafer alignment control before and after bonding. The bonding quality of wafers and dies should also be characterised. Parameters to be considered at die level include curvature, surface roughness and flatness which might need to be coupled with wafer level information. Wafer/die contamination before bonding, interface defectivity and adhesion after bonding, and local stress and thermal dissipation at the interface of bonding wafers and dies should also be considered.
4. To provide traceable metrology for thickness uniformity and surface quality control in wafer/die thinning (in the presence of circuits) and techniques for measuring stress relaxation, crystalline defects and surface contamination.
5. To engage with the semiconductor industry and others to facilitate the take up of the technology and measurement infrastructure developed by the project, to support the development of new, innovative products utilising 3D-stacked ICs, thereby enhancing the competitiveness of EU industry.

Proposers shall give priority to work that meets documented industrial needs and include measures to support transfer into industry by cooperation and by standardisation. An active involvement of industrial stakeholders is expected in order to align the project with their needs – both through project steering boards and participation in the research activities.

Proposers should establish the current state of the art, and explain how their proposed project goes beyond this and EMRP JRP NEW01 (TReND) 'Traceable characterisation of nanostructured devices'.

EURAMET expects the average EU Contribution for the selected JRPs to be 1.5 M€, and has defined an upper limit of 1.8 M€ for any project.

EURAMET also expects the EU Contribution to the external funded partners to not exceed 30 % of the total EU Contribution to the project. Any deviation from this must be justified.

Any industrial partners that will receive significant benefit from the results of the proposed project are expected to be unfunded partners.

Potential Impact

Proposals must demonstrate adequate and appropriate participation/links to the "end user" community, describing how the project partners will engage with relevant communities during the project to facilitate knowledge transfer and accelerate the uptake of project outputs. Evidence of support from the "end user" community (e.g. letters of support) is also encouraged.

You should detail how your JRP results are going to:

- Address the SRT objectives and deliver solutions to the documented needs,
- Drive innovation in industrial production and facilitate new or significantly improved products through exploiting top-level metrological technology,
- Improve the competitiveness of EU industry,
- Feed into the development of urgent documentary standards through appropriate standards bodies,
- Transfer knowledge to the semiconductor and other sectors.

You should detail other impacts of your proposed JRP as specified in the document "Guide 4: Writing Joint Research Projects"

You should also detail how your approach to realising the objectives will further the aim of EMPIR to develop a coherent approach at the European level in the field of metrology and include the best available contributions from across the metrology community. Specifically the opportunities for:

- improvement of the efficiency of use of available resources to better meet metrological needs and to assure the traceability of national standards
- the metrology capacity of EURAMET Member States whose metrology programmes are at an early stage of development to be increased
- organisations other than NMIs and DIs to be involved in the work

Time-scale

The project should be of up to 3 years duration.

Additional information

The references were provided by PRT submitters; proposers should therefore establish the relevance of any references.

[1] "A European Industrial Strategic Roadmap for Micro- and Nano-Electronic Components and Systems" http://ec.europa.eu/digital-agenda/en/news/european-industrial-strategic-roadmap-micro-and-nano-electronic-components-and-systems

[2] For some integration schema, TSV technology is already a reality in the market, enabling products such as CMOS imagers, FPGA and MEMS.

[3] Poupon G. et al Proceedings of the IEEE conference, vol. 97, No. 1 60-69 (2009).

[4] Ramm et al. ESSCIRC - 36th European Solid State Circuits Conference 9-16 (2010).

[5] International Technology Roadmap for Semiconductors– ITRS 2012.