Title: Metrology for advanced energy-saving technology in next-generation electronics applications

Abstract

In 2020, 5G telecommunications will be rolled out across Europe and it is expected that the Internet of Things will consist of 50 billion connected devices. This will strongly increase the demand for energy due to the continuous power consumption of the electronic devices needed to deliver these next-generation technologies. To reduce power consumption at device level, research in metrology is needed to support the development of a new class of materials, optimise the energy consumption of device components and improve the power measurement of electronic systems. With more accurate and traceable measurements of power losses and material properties European industries (such as the telecommunications industry) will be able to optimise the design of the devices and facilitate more efficient electronic components thereby advancing energy-saving in next generation electronic applications.

Keywords

Next-generation electronics, telecommunications, electronic power consumption, ultra-low power, high frequency electronics, nano material characterisation, energy efficient materials and devices.

Background to the Metrological Challenges

The energy consumption during standby mode on electronic devices can reach up to 22 % of all appliance consumption, and 9 % to 16 % of total residential consumption and therefore the increase in the number of wireless devices per household, driven by the internet of things applications and 5G telecommunications, will have a strong impact on this energy usage. As a result, the significant increase of wireless electronic devices has to be balanced by a dramatic reduction in power consumption.

Three types of novel ultra-low power device electronics have been developed based on the following field-effect transistor (FET) principles; energy filtering, internal potential step-up and internal transduction, however none of these devices have the switching times and low-voltages required. The PiezoElectronic transistor (PET) is another novel device concept which uses the energy filtering and internal transduction principles to convert an electrical signal to acoustic form, enhance it via mechanical design, and reconvert to electrical form. Switching times of a few ps at voltages of order 0.1 V are expected at 30 nm length scales and studies have shown that the PET can operate at 1/50 the energy of the FET at the same speed (4 GHz) and is therefore much better positioned to replace the FET in nearly all computer applications.

To support the development of these novel classes of devices the characterisation of their material (e.g. stress and strain), electrical (e.g. electric field, impedance and capacitance) and magnetic (e.g. magnetic field) properties measurements is crucial to overcome power and thermal issues while also increasing the CPU frequency and extend memory capabilities and benefit the next class of low power device. Traceable, in-situ and in operandi forces of micro Newtons, electric fields of 4 MV/cm and magnetic fields of up to 2 T are now required. To measure impedance Alternating Current (AC) or Direct Current (DC) measuring instruments associated with 4-probe manipulators can be used but lack traceability and impedance standards at the required nanoscale. At the present time, there is no traceability for capacitance measurements in the atto-farad range. Comparisons with other techniques, e.g. the use of a capacitance bridge connected with an AFM need to be investigated.

One of the key factors to optimise energy consumption of electronic components is an understanding of how to measure loss in switching devices (including transistors) and minimising the power used by these devices will be a critical operating metric to ensure their suitability in, and applicability to, next generation technologies.

MOSFET- and IGBT-based switching devices have losses caused by their parasitic elements. Switching losses have time dependent characteristics that can be measured and characterised using an oscilloscope for the synchronous measurement of the voltage and the current. Currently power efficiency is measured with an uncertainty of 2 %. Emerging switching devices that operate at radio and microwave frequencies could largely improve the efficiency by increasing the switching frequency. Developing appropriate time-domain methods and algorithms for measuring switching losses for high-speed switching devices and the corresponding reference standards provides a straightforward approach to being able to improve energy efficiency SMPS while assuring compliance with standards.

Signal power detectors are widely used in wireless communication systems, which often use automatic gain control (AGC) circuits to minimise power consumption and to optimise system performance. However, because of the scaling reduction and increase of density of components, power and thermal measurements are becoming increasingly integrated by many semiconductor suppliers at chip level. During the last decade, on-chip power sensors dedicated to wireless devices have been developed using CMOS technology. Depending on the antenna impedances, the error in detected power ranges from ±0.1 dB to ±0.6 dB. The minimum detectable signal is approximately -33 dBm at 900 MHz and -25 dBm at 2.4 GHz; the dynamic range is typically 30 dB. The detectors have to exhibit a wideband frequency response and high sensitivity for measuring low power levels. There is a clear need to improve the accuracy of on-chip detectors as well as calibration techniques to accurately characterise these sensors.

Objectives

Proposers should address the objectives stated below, which are based on the PRT submissions. Proposers may identify amendments to the objectives or choose to address a subset of them in order to maximise the overall impact, or address budgetary or scientific / technical constraints, but the reasons for this should be clearly stated in the protocol.

The JRP shall focus on the traceable measurement and characterisation of ultra-low power and high frequency energy efficient electronic devices.

The specific objectives are

1. To develop nano-metrology adapted to the new class of materials proposed for the next generation of ultra-low power energy-efficient devices. These measurements will include impedance measurements (in the atto-farad and micro-ohm regions), piezo-electric/piezo-resistive stress (200 MPa) and strain (0.02 %) responses to the application of electric (up to 4 MV/cm) and magnetic fields (up to 2 T), as well as temperature and pressure in the range encountered in electronic devices.
2. To develop frequency and time-domain techniques for the simultaneous measurement of dynamic thermal profiles, electro-magnetic field sensing, DC electrical power consumption and RF operating waveforms for a wide range of electronic components (operating in-situ, under realistic conditions). The uncertainty in the measurement of the power efficiency will be reduced to less than 1 %.
3. To develop embedded sensors and the associated calibration and measurement techniques to accurately measure power consumption of wireless systems (mobile phones, tablets and connected devices) and to improve the effectiveness of analog and RF tests of components and systems. The power measurement techniques will be able to characterise and calibrate on-chip power sensors with an uncertainty target of less than 10 µW.
4. To facilitate the take up of the technology and measurement infrastructure developed in the project by the measurement supply chain (accredited laboratories), standards developing organisations (ISO) and end users (semi-conductor industry, telecommunications sector)."

These objectives will require large-scale approaches that are beyond the capabilities of single National Metrology Institutes and Designated Institutes. To enhance the impact of the research, the involvement of the appropriate user community such as industry, standardisation and regulatory bodies is strongly recommended, both prior to and during methodology development.

Proposers should establish the current state of the art, and explain how their proposed research goes beyond this.

EURAMET expects the average EU Contribution for the selected JRPs in this TP to be 2.0 M€, and has defined an upper limit of 2.3 M€ for this project.

EURAMET also expects the EU Contribution to the external funded partners to not exceed 35 % of the total EU Contribution to the project.

Any industrial partners that will receive significant benefit from the results of the proposed project are expected to be unfunded partners.

Potential Impact

Proposals must demonstrate adequate and appropriate participation/links to the “end user” community, describing how the project partners will engage with relevant communities during the project to facilitate knowledge transfer and accelerate the uptake of project outputs. Evidence of support from the “end user” community (e.g. letters of support) is also encouraged.

You should detail how your JRP results are going to:

- Address the SRT objectives and deliver solutions to the documented needs,
- Feed into the development of urgent documentary standards through appropriate standards bodies,
- Transfer knowledge to the telecommunications sector.

You should detail other impacts of your proposed JRP as specified in the document “Guide 4: Writing Joint Research Projects (JRPs)”

You should also detail how your approach to realising the objectives will further the aim of EMPIR to develop a coherent approach at the European level in the field of metrology and include the best available contributions from across the metrology community. Specifically the opportunities for:

- improvement of the efficiency of use of available resources to better meet metrological needs and to assure the traceability of national standards
- the metrology capacity of EURAMET Member States whose metrology programmes are at an early stage of development to be increased
- organisations other than NMIs and DIs to be involved in the work

Time-scale

The project should be of up to 3 years duration.