



Publishable Summary for 22RPT02 True8DIGIT Towards a true 8-digit digitiser

Overview

This project addresses the development of a digitiser based on state-of-the-art analogue-to-digital converters (ADCs), operating from direct current (DC) to 100 kHz, meeting the demands for linearity, noise, and overall accuracy of high-level measurement applications that cannot be met using currently available digitisers. In this project research on the key techniques and technologies needed to underpin a follow-up full-scale project will be performed. An important aim is to provide research capacity building opportunities for developing NMIs/DIs on the design and characterisation of electronic measuring devices needed for a wide variety of interdisciplinary metrological challenges such as state-of-the-art DC measurements and advanced digital sampling techniques. This will enable these NMIs to join future full-scale projects.

Need

High resolution digitisers, used to convert electrical signals into digital form, which were first developed for metrology applications are now used for signal analysis in a wide range of applications including those in the automotive, aerospace, communications and medical fields. Extending the performance of digitisers beyond the current state-of-the-art, to deliver accuracy levels below the part per million level, will widen the range of signals accessible to traceable, reliable, and accurate measurement.

The core element of a digitiser is the analogue-to-digital converter (ADC). In 2016, the global analogue-to-digital converters market was valued at \$2.3 billion and is projected to double in value by 2027 growing at a compound annual growth rate (CAGR) of 6.7 % from 2019 to 2027. Dual-slope and $\Delta\Sigma$ ADCs share approximately 5 % and 20 % of the market, respectively. While high accuracy ADCs have traditionally found applications in the instrumentation and research arenas, they are rapidly and aggressively entering the medical (MRI, digital radiography, CT, ultrasonography), industrial and consumer (audio) markets.

Analogue-to-digital conversion is arguably the most widely used measurement technology worldwide, employed in almost all communication, smart (IoT) sensors, measuring devices and instrumentation regardless of the application area, up to redefined SI unit realisations. This is due to ADCs ability to provide the most straightforward conversion of analogue information obtained by sensors and transducers to its digital representation, which can then be further integrated into our increasingly digital world. The applications of digitisers often call for state-of-the-art capabilities across all performance parameters and there exist numerous examples in literature of attempts to optimise the performance of the best commercially available digitising solutions.

This project will extend the state-of-the-art in digitiser performance by using mixed technologies, mixed ADC architectures, powerful post-processing, and metrology class measurements to validate performance during all development steps. This will avoid the design compromises required for a full function digital multimeter on the one hand, and the fabrication challenges of an integrated circuit ADC on the other (such as power or size limitations, components price, chip area etc.). Such a development is a complex undertaking; therefore, this project proposes a two-step approach, (i) a capacity building project and (ii) a following full-scale JRP (in 2025 IEM call) to develop a functional metrology grade digitiser with a performance exceeding the current state-of-the-art.

Application fields for a digitiser with improved performance include, but are not limited to, audio, seismology, geographic surveying, industrial instrumentation and high-precision current control for accelerator magnets. Applications requiring novel digitiser solutions range from testing audio equipment, conversion of signals from high dynamic range seismic sensors, pressure and force gauges, weight cells, resistive thermometers and

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European Partnership



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thermocouples, as well as superconducting quantum interferometers (SQUIDs), particle accelerator beam instrumentation, coil based magnetic measurements and quench detection in superconducting magnets. All these applications require one or more of the following characteristics which will be focus of the research: extremely high intrinsic dynamic range, low distortion, low noise, excellent stability and excellent linearity.

Objectives

The overall objective of the project is to perform bottom-up development and research underpinning the development of a digitiser featuring state-of-the-art performance, whose performance exceeds that of currently available digital multimeters (DMMs), digitisers or analogue-to-digital converters (ADCs).

The specific objectives are:

1. To identify at least 2 novel metrology grade ADC architectures for the DC to 100 kHz frequency band and develop comprehensive digital models covering integrating ADC (IADC), Sigma-Delta ($\Delta\Sigma$) and at least 1 mixed design. The models will include first and second order error mechanisms. This includes identifying key performance targets such as measurement error below 1 part per million, comparing the performance of the ADC architectures, and mitigating and/or compensating for their non-ideal behaviour by means of simulations.
2. To assess at least 2 designs for novel amplifiers (composite operational amplifiers (COPAs)) for integrator and front-end digitiser circuitry with zero drift, extremely high gain, low noise and error below 1 ppm, and to develop the metrological tools to evaluate the amplifier's performance. Additionally, to identify metrological methods for characterisation of resistors and capacitors for the amplifier's stability, tracking and nonlinear behaviour down to and below -120 dB total harmonic distortion (THD) and electronic switches for their injection currents and transients' stability.
3. To design and develop an ultra-quiet and stable low noise power supply, supplied from the mains supply but with negligible line interference noise, and applicable for all voltage and current spans needed by the metrology grade ADC architectures identified in objective 1.
4. To develop a precision (< 50 ps jitter) timing solution for the ADC architectures identified in objective 1, with a galvanically isolated external trigger, lock-in and internal clock frequency output, and to develop the metrological tools such as jitter and synchronisation measurement to evaluate ADC architectures' timing performance.
5. To facilitate the take up and long-term operation of the capabilities, technology and measurement infrastructure developed in the project by the measurement supply chain (NMIs/DIs, calibration and testing laboratories), and end users (e.g. electrical power generators, manufacturers of medical imaging devices, ADC and DMM industry). The approach will be discussed within the consortium and with other EURAMET NMIs/DIs, EURAMET TCs or EMNs, to ensure that a coordinated and optimised approach to the development of traceability in this field is developed for Europe as a whole.

Progress beyond the state of the art and results

Novel metrology grade ADC architectures

For high accuracy sampling measurements, a limited number of high-end digital multimeters and commercial digitisers are currently available in the market. However, their performance limits progress in precision low frequency applications.

This project will deliver key solutions and proofs of concept that will be used to underpin a follow-up project to develop a fully operational digitiser with improved linearity, dynamic range and accuracy. Development of new hybrid topologies with different ADC architectures will be supplemented with a parallel SAR architecture and the use of an ultra-pure sine wave or multi-tone sources will be implemented to improve digitiser linearity in AC regime.

Characterisation of composite operational amplifiers, linear components and switches

A key component in both IADC and $\Sigma\Delta$ ADC is the operational amplifier (OPA) which performs integration via a feedback capacitor. Single commercial OPAs do not meet the requirements for use as in a state-of-the-art IADC integrator or for zero-drift front-end design.

This project will deliver new topologies for composite operational amplifiers (COPAs) and build prototypes with superior performance to demonstrate that the current performance limitations of integrating and $\Sigma\Delta$ ADCs can

be overcome. Measurement techniques will be developed to characterise prototypes of COPAs. A different design of COPA will be delivered for a front-end circuitry with the lowest possible $1/f$ noise down to mHz and with high linearity and stability to cater for signal frequencies up to 100 kHz.

A precision ADC relies critically on selected linear components and switches that define its performance. However, characterisation of potential imperfections that are known in theory is lacking due to the considerable metrological challenge involved.

This project will deliver measurement techniques to characterise nonlinear behaviour of capacitors and resistors of different construction types and materials to the level required by the demanding objectives in this project. Switches will be tested for correct timing and charge injection repeatability and stability. Test beds will be constructed to isolate unwanted influences. Results will be used to update the models and determine their effect on the modelled ADC performance.

Ultra-quiet, stable and line interference free power supply

Power line interference, once introduced in the instrumentation is practically impossible to eliminate and consequently these interferences have a negative impact on precision sampling measurements. Available DC-DC supplies today with multiple isolations between the input and output can achieve lower leakage currents than transformer-based power supplies, but are limited in achievable output currents. Hence, the most demanding measurements require the use of batteries as a power source despite the limitation of their restricted operating duration.

This project will develop a novel power supply solution with insignificant line related interferences while allowing continuous operation. Potential malfunction identification and protection will be incorporated to protect sensitive loads.

Precision timing solution for ADC architectures

Accurate timing is essential in IADC and $\Delta\Sigma$ ADC designs, while perfect synchronisation is required for precision sampling measurements. Currently, no IADC or $\Delta\Sigma$ digitisers provide for true synchronisation.

This project will deliver a timing solution including low jitter multiple external triggers, lock-in and synchronisation with 100 MHz clock system frequency and galvanic isolation. This timing solution will provide necessary tools for a true synchronisation, that would be applicable also for new IADC architecture.

Outcomes and Impact

The outcome of this project targets three pillars: (i) to provide necessary proof-of-concept on key solutions to underpin a follow-up project in the 2025 IEM call; (ii) to provide solutions directly applicable to precision instrumentation; and (iii) to build research capacity in the developing NMIs/DIs that participate, thus enabling them to join a following full-scale project and any other related project with their acquired research capabilities.

Outcomes for industrial and other user communities

Industrial end users and stakeholders will directly benefit from the project outputs, such as advanced instrumentation with interference-free power supplies, cost effective selection of passive components for sensor/transducers and instrumentation, as well as precision isolated timing solutions for synchronised measurement systems. The project will provide key techniques and develop technologies to improve available state-of-the-art digitiser performance. An improved dynamic range would benefit seismology and geophysical surveying, where seismic sensors already provide a signal with such high dynamic range that even existing high-resolution digitisers present a bottleneck in the acquisition system.

This project will directly liaise with industrial stakeholders via the formation of a stakeholder committee. This group will include representatives from instrument and DAQ manufacturers, test and calibration service providers, chip manufacturers and research institutes, and will help the project's results to directly impact such representatives.

This project will also produce and publish two reports for end-users:

- Report on characterisation of non-linear effects in resistors and capacitors and stability of residual effects in switches.
- Report on characterisation of timing and synchronisation solution

The project's outcomes will be disseminated to instrument and data acquisition (DAQ) manufacturers and calibration laboratories by organising at least one international workshop aimed at collaborators and stakeholders, where key developed solutions will be presented, targeted to precision digitising, their wider applicability and impact to precision instrumentation and measurements.

Outcomes for the metrology and scientific communities

The project will improve and extend electrical sampling metrology for signals from DC to frequencies beyond the audio range, leading to innovation in the development and improvement of the precision measuring systems and instrumentation. The project's outcomes will provide the basis for improvements in the realisation of new SI units, and applications requiring precise synchronisation and amplitude/phase accuracy at or below the 1 ppm level, such as power and energy measurement, smart grid and power quality reference instrumentation calibrations, impedance bridges, AC Josephson, as well as in other measurement fields such as accurate readouts for highly stable temperature sensors. This will have a significant impact on calibration laboratories and their customers.

In the area of digitisation and instrumentation, knowledge transfer from experienced NMIs to those less experienced on how to benefit from digitisation and how to design precision measurement systems will be highly beneficial.

The scientific community will benefit from improved readout from sensors, especially from intrinsically low-noise devices like superconducting magnetometers, particle accelerator beam instrumentation, digital integrators for detecting coil-based magnetic measurements and quench detection in superconducting magnets. Such applications are often driven by highly specific requirements that cannot be summarised, but they all call for a best achievable linearity and stability in the final data conversion stage.

Major scientific impact will be provided through the publication of project results in scientific journals and presentations at key conferences. The project will disseminate all key results directly via relevant EURAMET technical committees and further to accredited calibration laboratories and scientific community via conference presentations, scientific publications, web page and appropriate social media outlets.

Outcomes for relevant standards

The project will investigate new test methods required for testing ADC performance beyond the current state-of-the-art for linearity and stability. This will impact IEEE standard 1241, and the consortium will communicate directly with IEEE committee TC10 as this is responsible for all IEEE ADC and DAC related standards. Dynamic performance testing will be developed through the use of ultra-pure sine wave and multi-tone sources. This will be relevant for IEC 60748-4-3, which covers dynamic criteria for analogue-to-digital converters. The consortium will liaise with IEC TC47 SC47A as this is the committee responsible for maintenance of this standard. This is also relevant to work being undertaken in IEC TC85 WG22.

Longer-term economic, social and environmental impacts

The technological environment in which science and industry operates depends, to a large extent, on our ability to measure phenomena in the physical world. To do this requires a sensor which converts the measured quantity into a measurable analogue signal and a digitiser which converts this signal into a number.

The majority of the processing of analogue signals now takes place in the digital domain. The improved digitisers envisaged in this, and a potential associated follow-on project will, in time, filter down to everyday applications such as medical diagnostics, energy conservation, security and the internet of things.

Improvements in the precision, speed and accuracy of digitisers over the years have allowed us to measure a wider range of quantities with ever greater sensitivity, with consequent benefits in fields such as manufacturing, medical diagnostics, smart electrical grids, energy conservation and environmental protection. Nonetheless, there is still a wide variety of signals, for example, in the fields of power quality, geophysics, acoustics, whose accurate measurement lies beyond the capability of even the best digitisers that are currently available. Improvements in ADCs, which provide the core element for digitisers, continue to be made. These advances can be exploited to produce metrology-grade digitisers, whose performance surpasses those of existing devices. To do this, every functional element of the digitiser, the signal conditioning block, the ADC itself, the power supply and the timing circuitry, must be optimised.

This project supports the long-term transition of EU toward digital transformation. The use of next-generation digitisers is a prerequisite for improved instrumentation and data acquisition systems, which are embedded in manufacturing for process control and quality assurance. Digital instrumentation is becoming standard in the power grid, where this project's outcomes in accuracy and timing will provide for an improved detection and localisation of critical events. New improved instrumentation is needed where the measurement of difficult-to-measure phenomena is necessary to make progress in the field.

List of publications

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This list is also available here: <https://www.euramet.org/repository/research-publications-repository-link/>

Project start date and duration:		01 June 2023, 36 months
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2. CMI, Czechia	11. CTU, Czechia	
3. FER, Croatia	12. INTI, Argentina	
4. INRIM, Italy	13. LeftRight, Slovenia	
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