Beyond Moore's Law

@ Politecnico of Torino

"Chilab – ITEM"

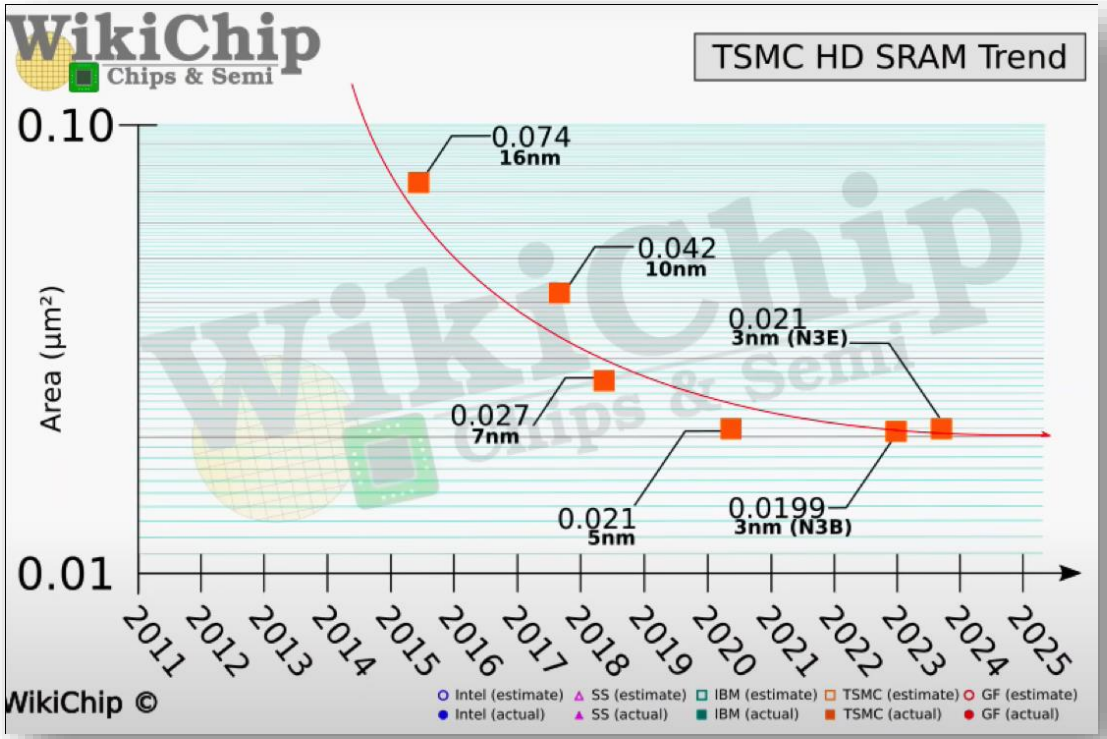
Prof. Luciano Scaltrito

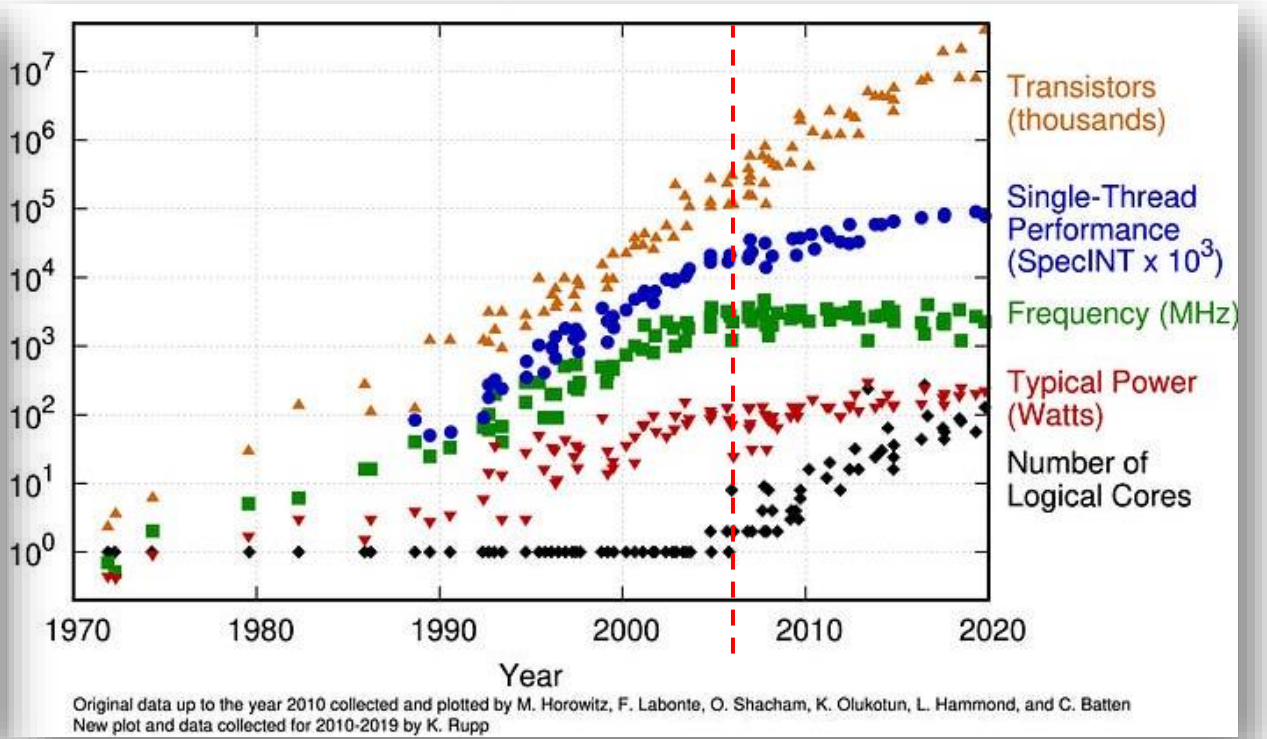
INRIM - 24TH October 2023

OUT LINE

- What is Moore’s law and is it still relevant in 2023?
- A technological point of view
- The route marked by PoliTo
- Chilab-ITEM Facilities
- Remarks and Conclusions

More than 50 Years of microprocessor trend data





There is an exponentially growing gap between our appetite for computation and what Moore's Law can deliver.

The open questions

Our civilization is based on computation, and …

“We must find technologies that transcend the current limitations of architecture and imagination”

Taking computing and communications beyond Moore's Law will require entirely new scientific, engineering, and conceptual frameworks, both for computing machines and for the algorithms and software that will run on them.

Take advantage of the ability to integrate MEMS (sensors and actuators) together with electronics in the same package

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Take advantage of the ability to integrate MEMS (sensors and actuators) together with electronics in the same package

Science and Engineering Beyond Moore's Law

Scientists are facing this big opportunity approaching the investigation following three main areas:

1) The basic science that underpins the hardware and software that are the tools of communications and computation;

2) **The engineering principles that drive the design of these tools**;

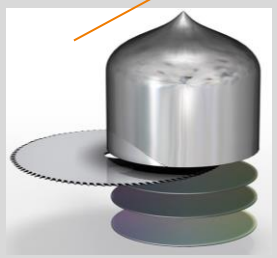
3) The computational framework that governs their utilization.

This is a big challenge for the entire microelectronics value chain!

Microelectronics value chain

PROCESS MACHINES MANUFACTURING

Raw materials



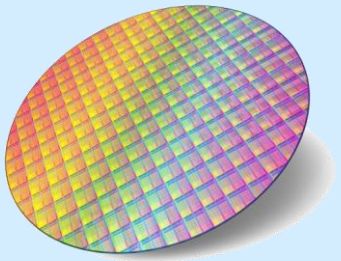
micheleangeletti.it

Si
GaN
SiC
GaAs

From sand to wafer

Front end Technology

(die/ SoC)

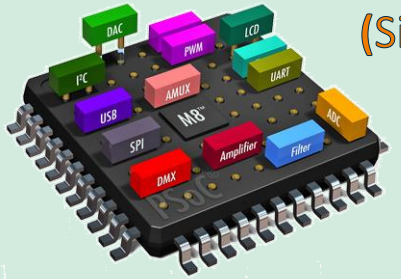


quora.com

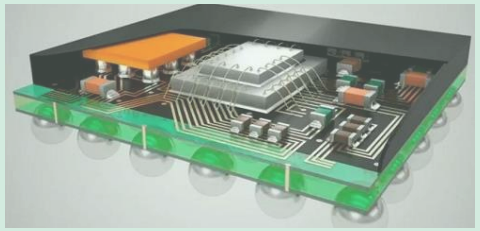
Dies testing

Back End Technology

microcontrollerslab.com



(SiP/Packaging)



utmel.com

systems testing

spea.com

final validation

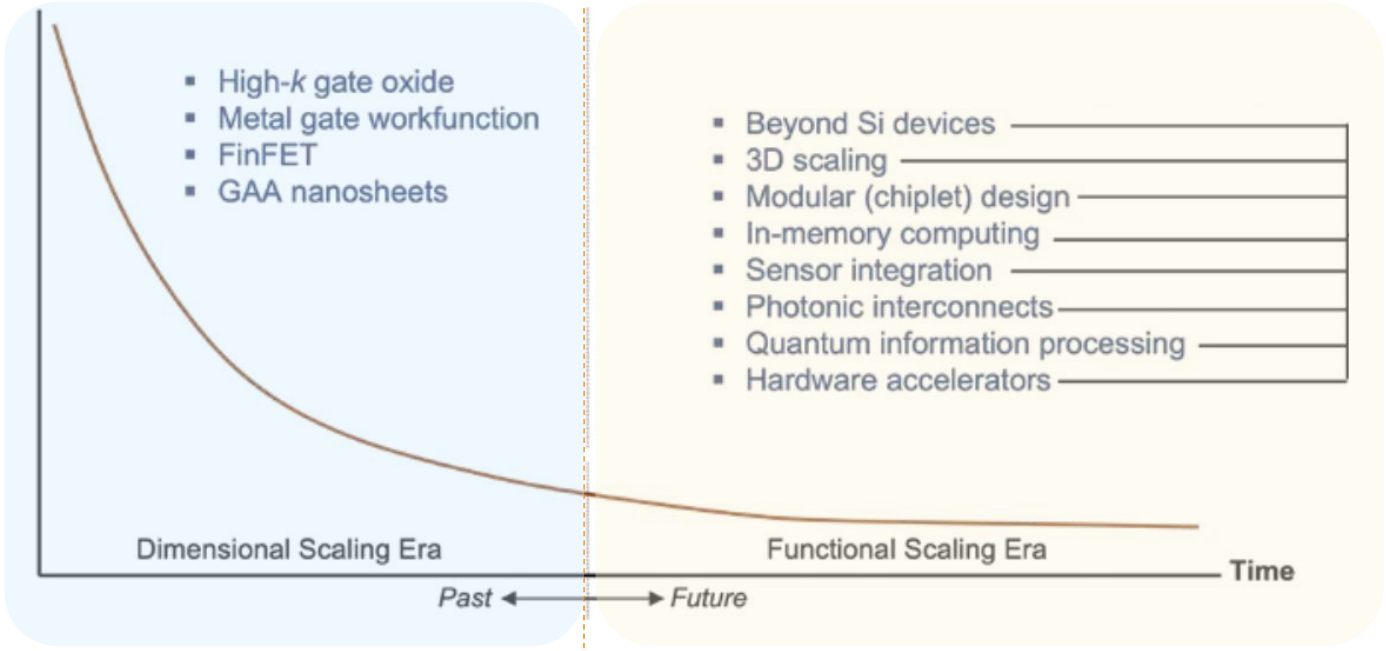
End users

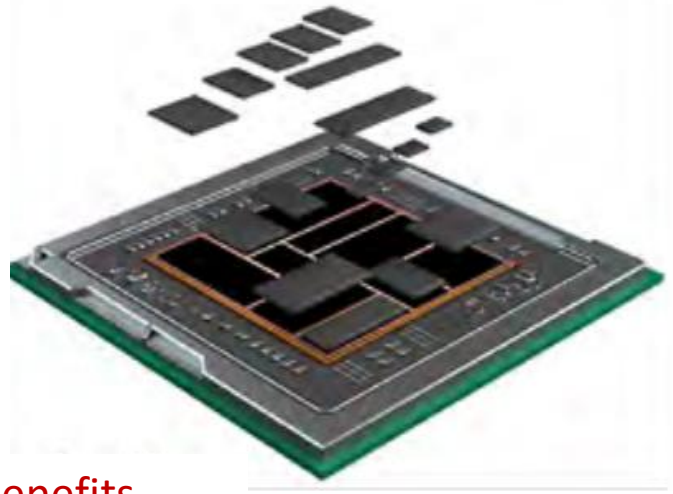
AUTOMATED TEST EQUIPMENT MANUFACTURING

The needs for science and technology breakthroughs

in **conventional**, **unconventional computing**, **power** and **high-frequency**

Minimum Feature Size — **Innovation Enablers** ❯ Heterogeneous Integration





Front end Technology

(Die / SoC)

Back End Technology

(SiP/Packaging)

Benefits

- **Mix and match design**
- **Shorter interconnects in 3D**
- **Escape from reticle limits**
- **Yield resiliency**
- **Faster time-to-market**

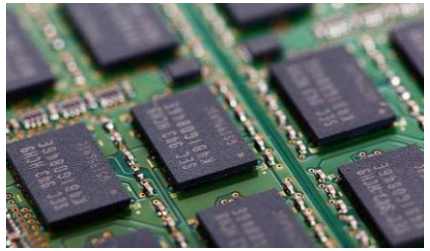
VT-ARC Virginia Tech Applied Research Corporation

Report, workshop held June 23-24, 2022, at the Basic Research Innovation Collaboration Center in Arlington, VA on the future of Microelectronics research.

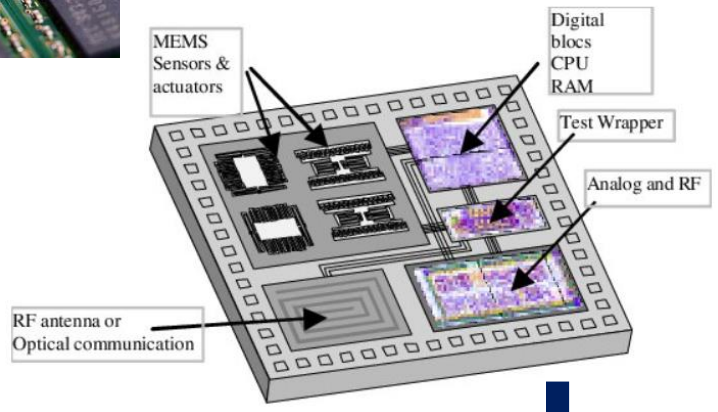
What does SoC mean?

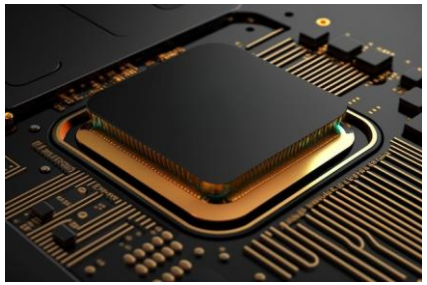
A System on Chip (SoC) integrates on a single chip all the electronics necessary for a specific device.

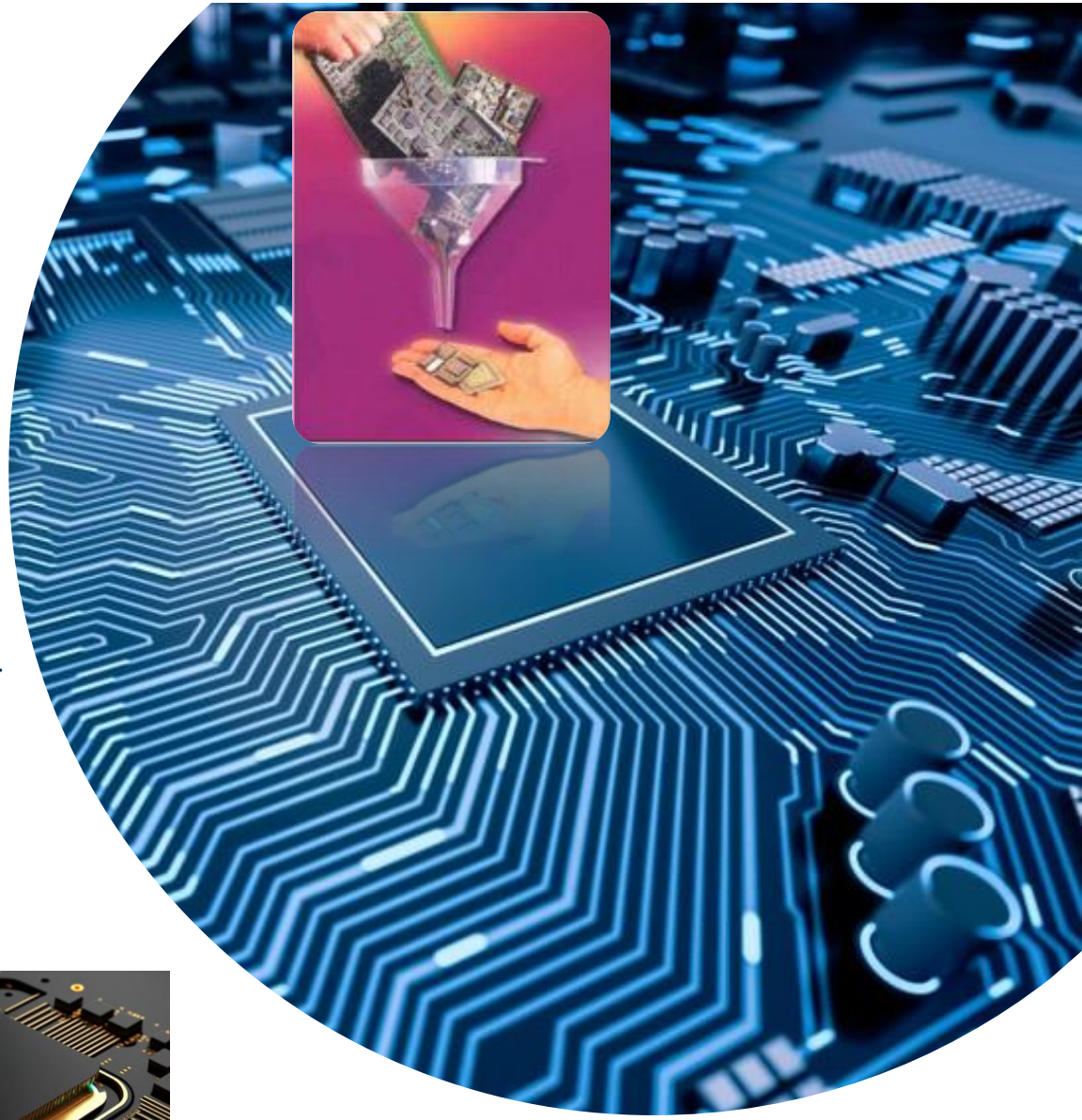
CPU, sensors, memories and other modules can be integrated.



In the mid-1990s, ASIC technology evolved from chip-set philosophy to an embedded-cores-based System-on-a-chip concept







SoC

Pros

- Reduce size, cost* and power consumption
- Increase performance

Cons

- Design (and debug) complexity
- Test complexity
- High cost*
- High time-to-market
- Limited fabrication flexibility (one semiconductor)

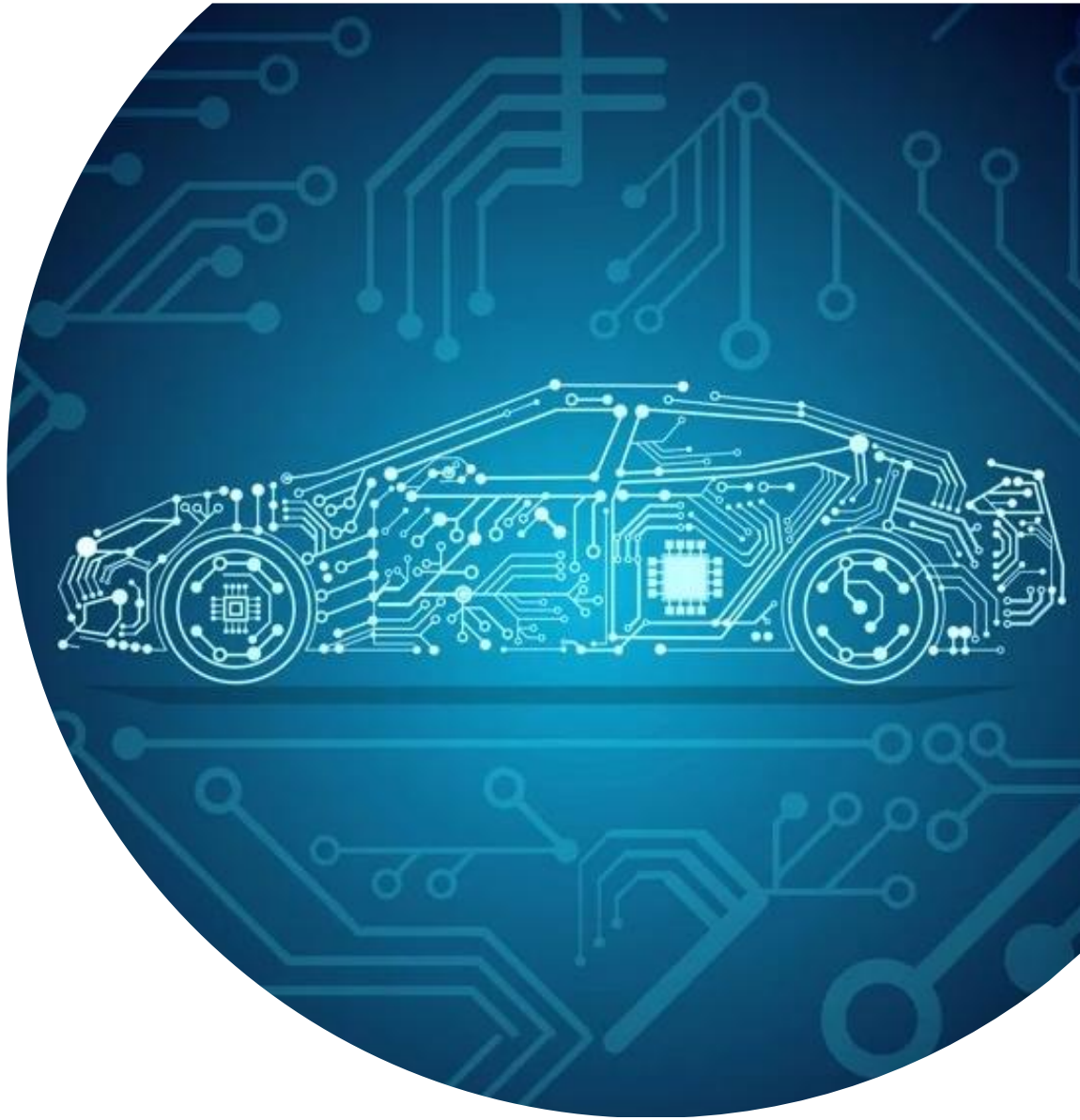
* Designing and manufacturing steps are very expensive.
For this reason, cost is a pro whenever the object can be mass-produced.

SoC Applications

SoCs have been applied to all mass-produced (due to high cost and long designing time), nano- and micro-, wearable devices.

Main field of application are:

- Mobile devices
- High-volume consumer electronics
- Automotive
- IoT
- Aerospace and Defence



Limits and further improvements of SoC

However, the miniaturization process is running up to the nanoscale (see for example Intel Core i9-13900K, 7 nm, Apple M2 Pro, 5 nm).

The limits are:

- Costs
- Rising of quantum phenomena

Is this the end of Moore's law? Yes but…

Some new strategies in terms of integration and packaging can be implemented in order to achieve new devices with increasingly high-performance

For example: 3DIC, SiP…

Three-Dimensional Integrated Circuits (3DIC)

Traditional SoCs are planar. However, 3D structures can be created assembling different layers of chip or directly created on the wafer.

There are different construction methods:

- Monolithic 3DIC
- Die-on-Wafer stacking
- Wafer-level stacking
- Chip stacking or Chip-on-Chip (CoC)

} Precursors of SiP

Paul D. Franzon 2021
NC State University

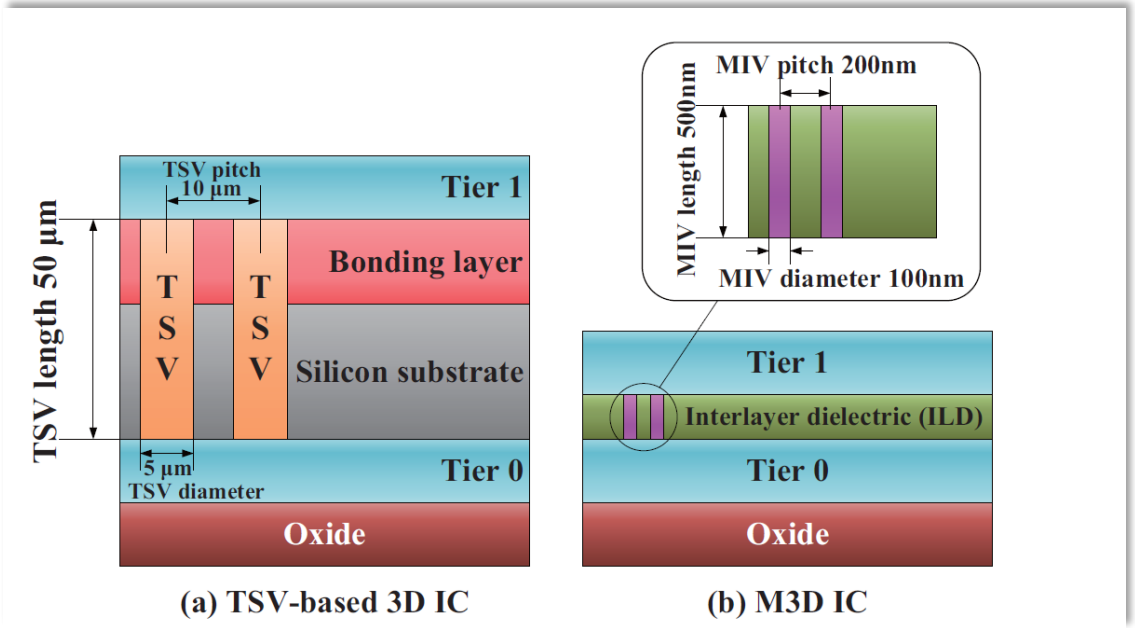
System in Package – SiP* → ***A new era of block-based processes*

3D-Chip stacking: TSV and MIV

In the past two decades, some improvements have been developed for (Chip stacking) such as Through Silicon Via (TSV). Nowadays technology, as discussed in previous slides, has reached the nanoscale for transistor's channel length. However, TSV are hundreds time bigger. This reduce the integration density and granularity introducing significant RC delay

Monolithic 3DIC mitigates a lot these phenomena using monolithic inter-tier vias (MIVs) that reach the nanoscale

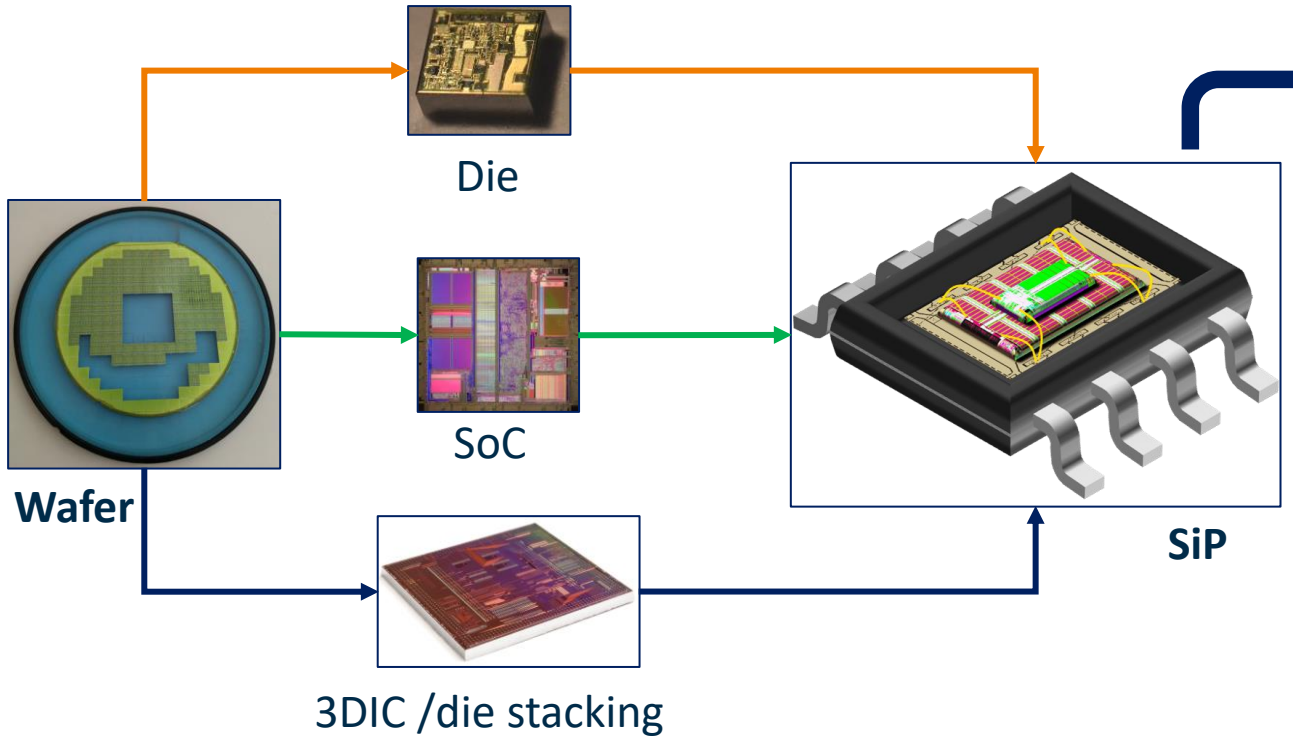
	TSV	MIV
Diameter	5 µm	100 nm
Length	50 µm	500 nm
Pitch	10 µm	200 nm
Resistance	35 mΩ	2 Ω
Capacitance	100 fF	0.1 fF



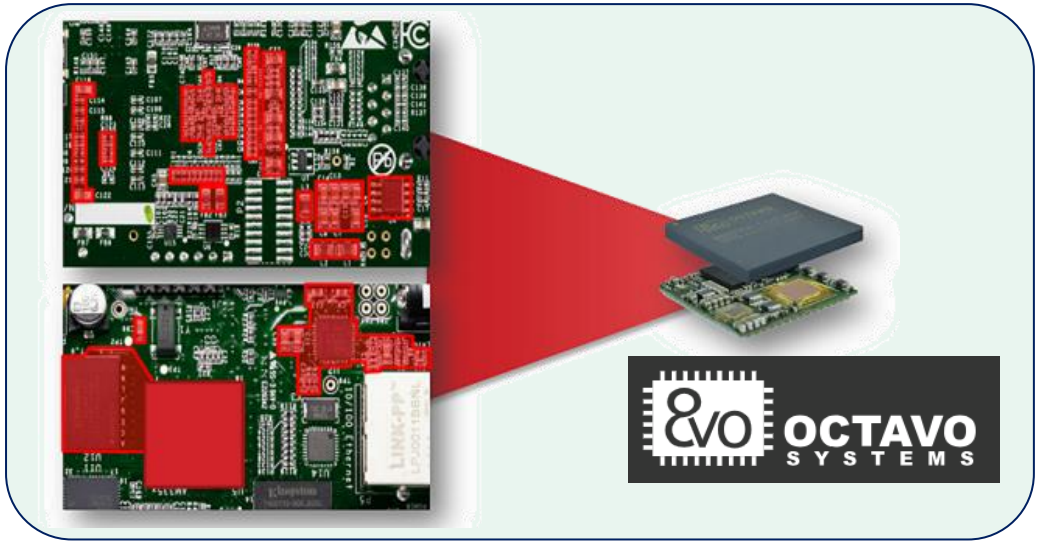
SiP (System-in-Package)

It refers to a system able to bundle multiple Integrated Circuits (ICs) and passive components (inductors, resistors, etc..) into a single package

Its development is strictly related to the **«Heterogeneous integration»** concept

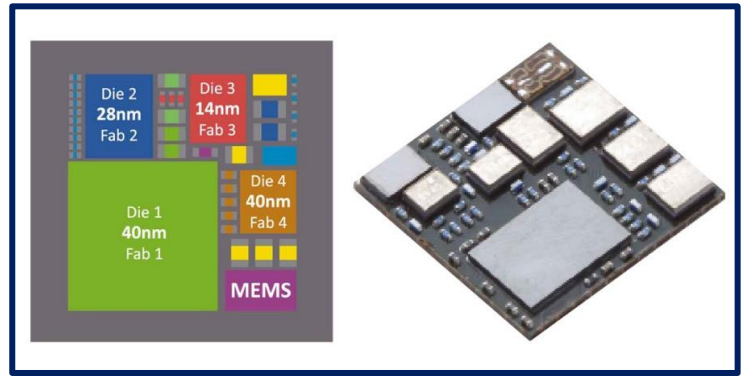


1. **Get you to market faster**
2. **Reduce the Size of your Design**
3. **Save you money**

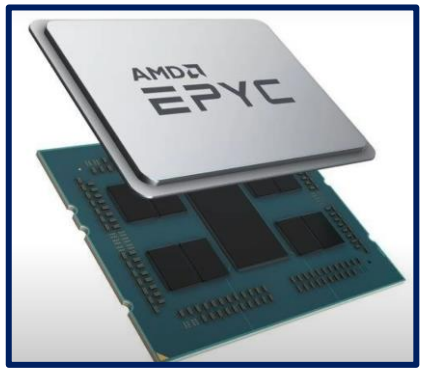


Heterogeneous Integration

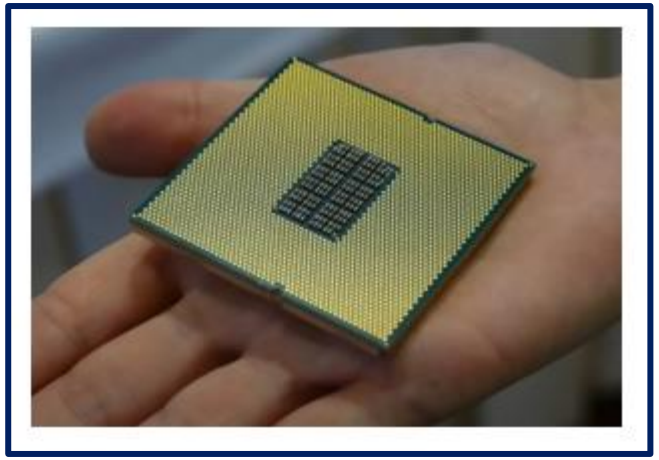
«**HI**» is the integration of separately manufactured components into a higher-level assembly that provides enhanced functionality and improved operating characteristics



Just a successful example

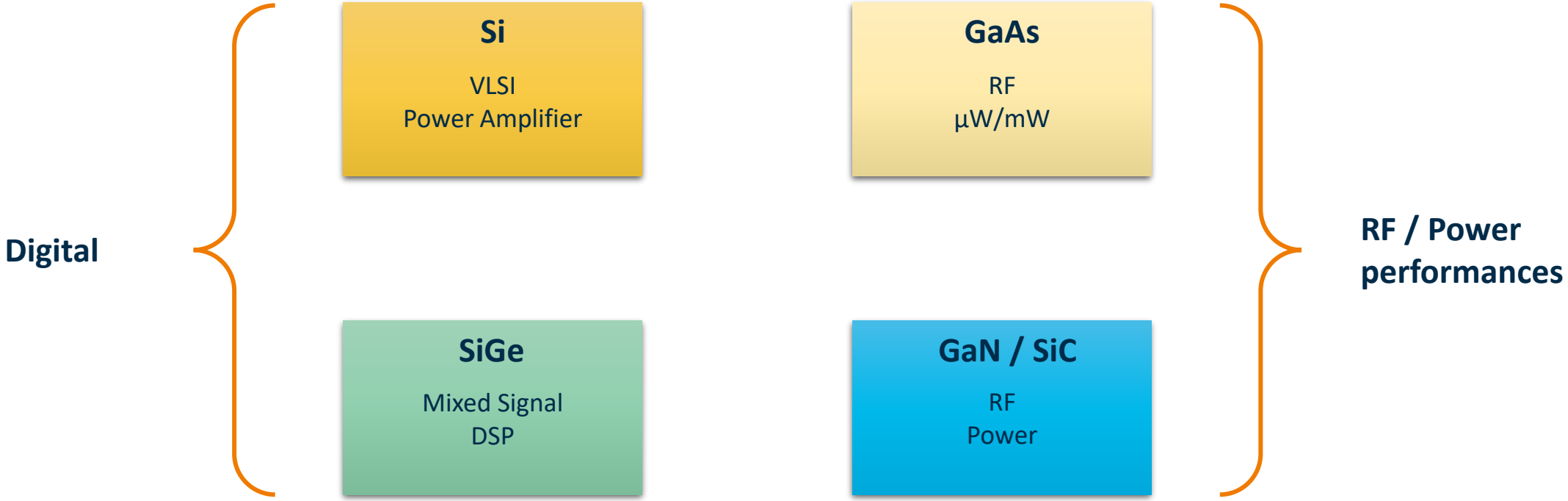


AMD – EPYC
CPU, code-named Naples
14nm process
777smm large



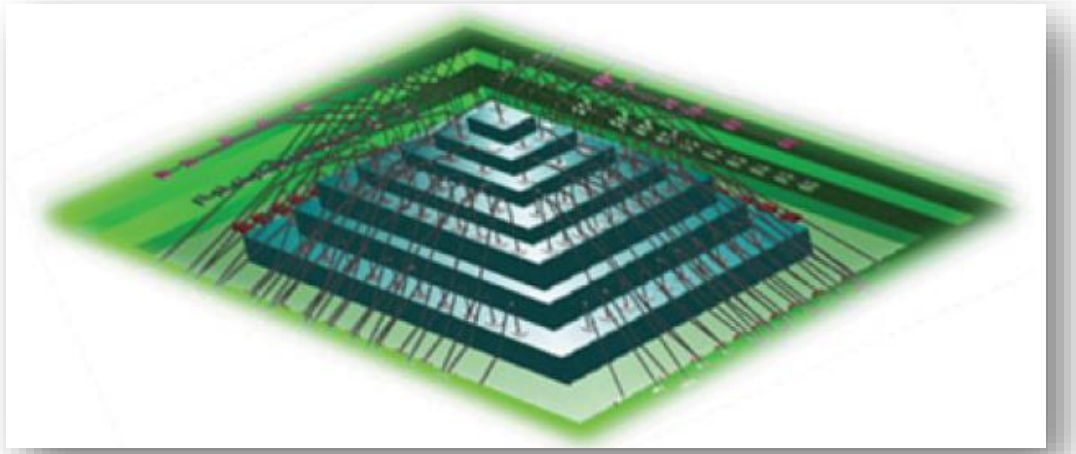
All semiconductors in SiP

The growing demand for the highest performances made necessary the use of more than a single technology



3DIC & SoC in SiP

So, stacking vertically two or more chips (Chip-stacking) it is possible to obtain the so-called 3D-SoC which, eventually, can also be part of a System in Package (SiP).



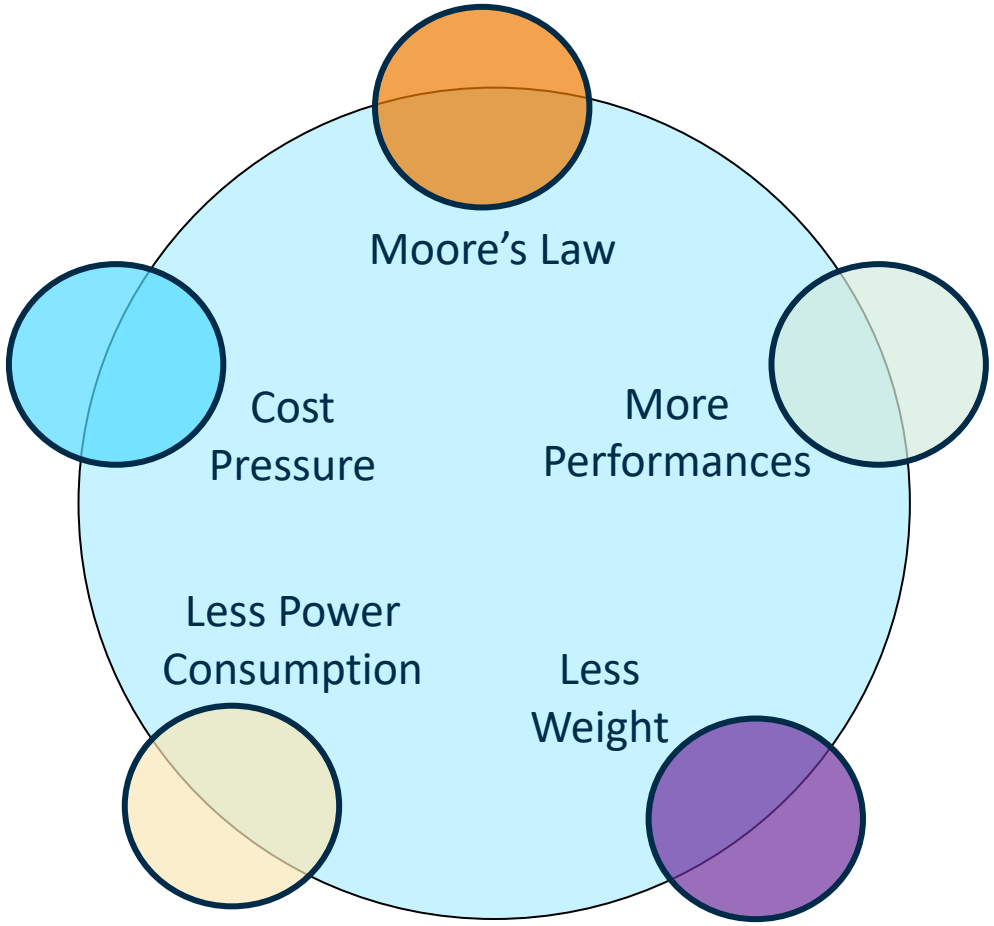
Chip-stacking

System in Package

Why SiP?

SiP is the best tradeoff of a combination of several factors

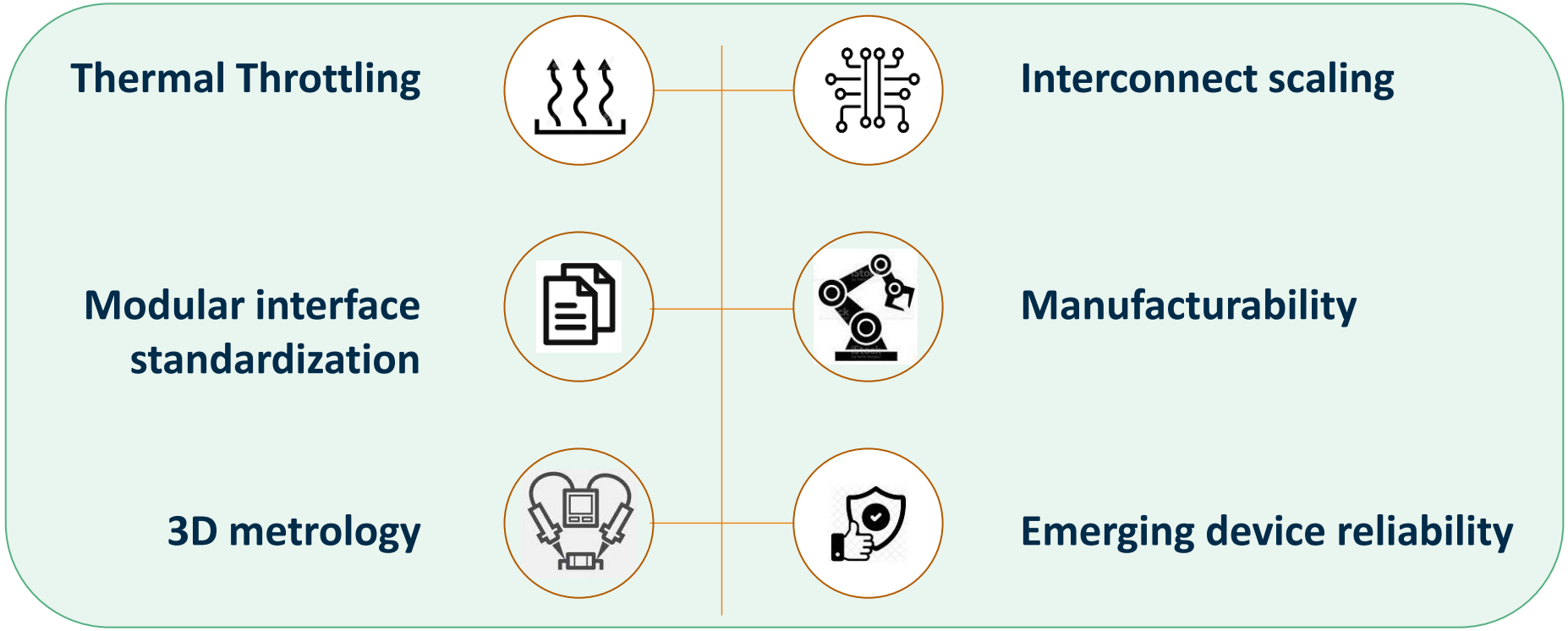
advantages



Scientific challenges to BEOL

Focusing on the composition of a SiP, the key elements are: **Materials**, **Interconnections**, **Encapsulation** and **Architecture Design.**

A complex issue to be treated synergically …



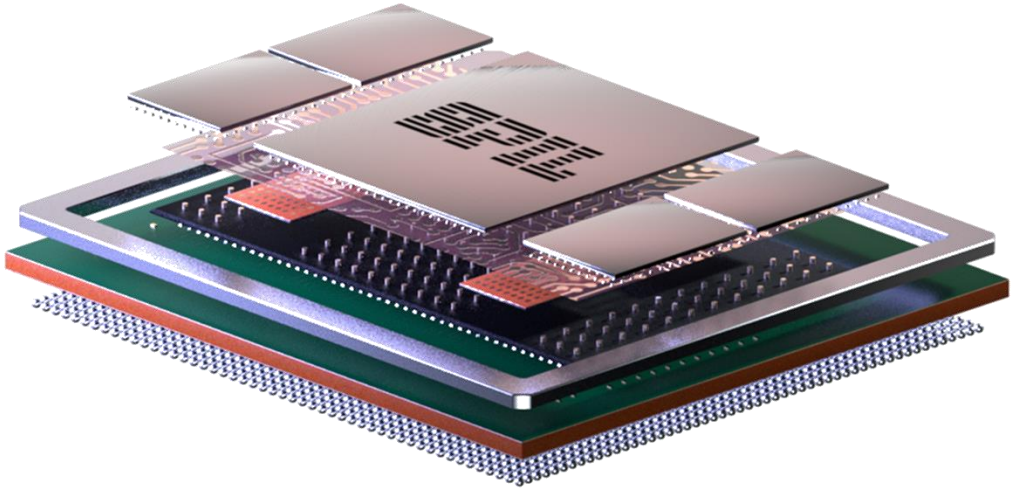
Co-design for heterogeneous integration (SiP)

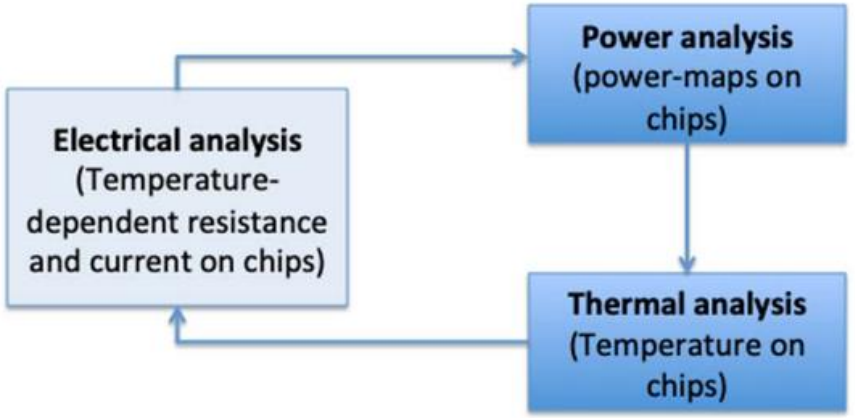
The emergence of new materials and devices with applications is expanding **for heterogeneous integration** and creating new opportunities for co-design in which multi-physics, multi-scale and multi-level analyses will provide the needed solutions.

- Heterogeneous integration need of a **parallel** and **integrated flow** for **design**, **processes** and **analysis optimization**.
- **Co-design addresses the discontinuity that exists between IC design and packaging**.

A team of designers is growing at Chilab-ITEM

Design of SiP – "Siemens Simcenter 3D**"**



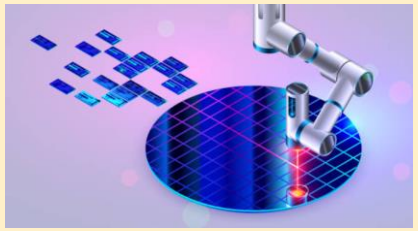


Heterogeneous Integration Roadmap 2021 Edition, Chapter 13 Co-Design

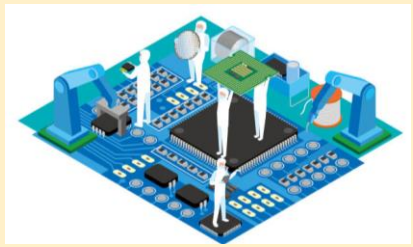
SiP - Process Flow available at Chilab-ITEM

Multiphysics simulation

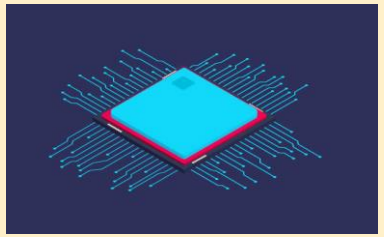
Interconnection



Laser dicing



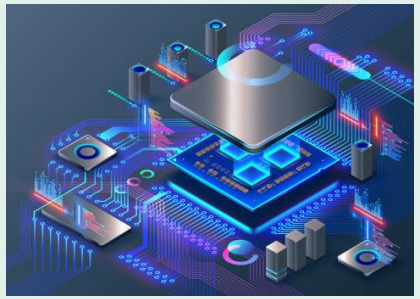
Pick and place



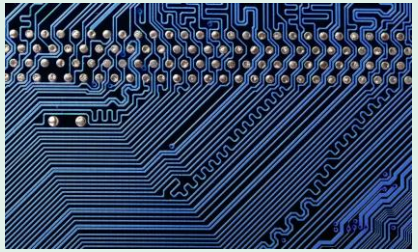
Wire bonder/Die bonder

Reflow oven

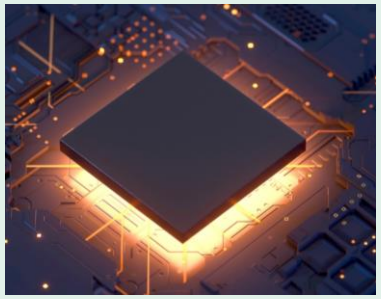
Packaging



Ceramic printing



Electronics printing



Polymer thermoforming

Laser welding

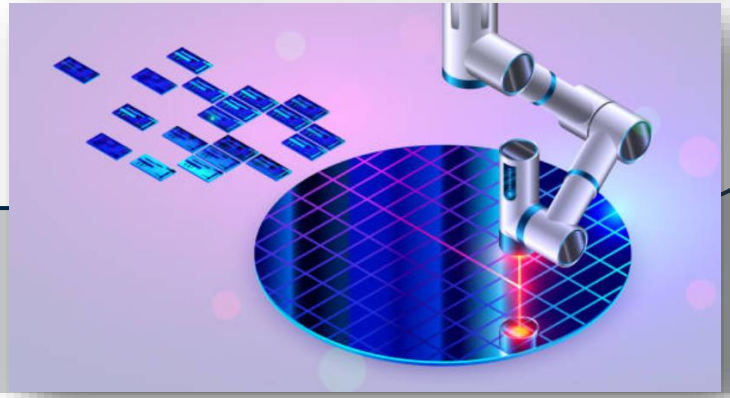
Thermal, electrical, morphological characterization

Laser Processing

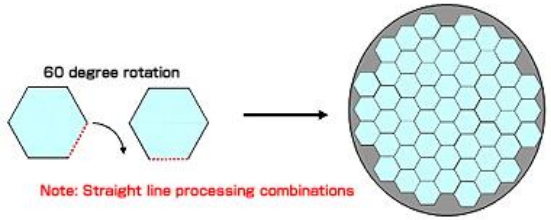
Laser dicing

Features

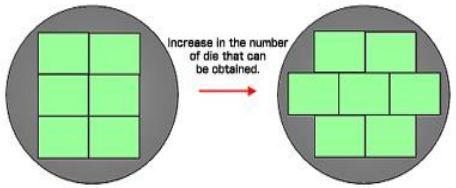
- ✓ Small heat affected zone & non-contact process
- ✓ Unrelated to workpieces hardness
- ✓ Streets etching down to 10 µm
- ✓ 3 in 1: ablation provides three processes by adjusting the laser depth:
  - scribing;
  - grooving;
  - full cut



Irregular shaped die



Die offset

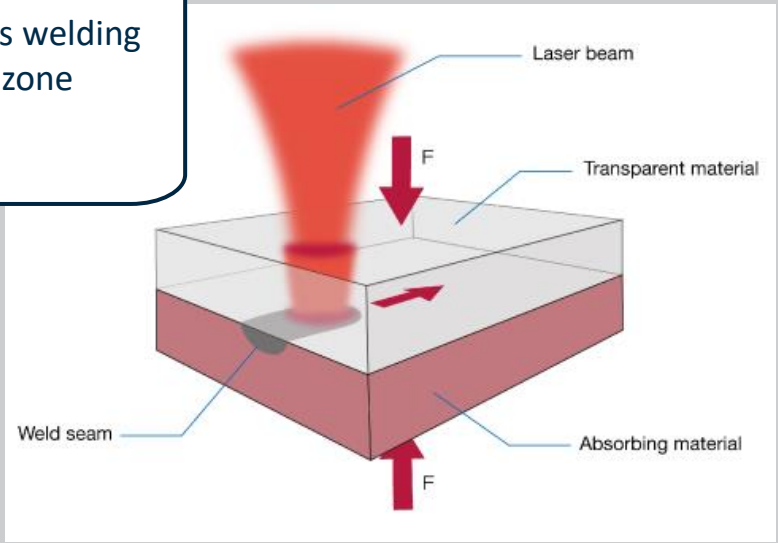


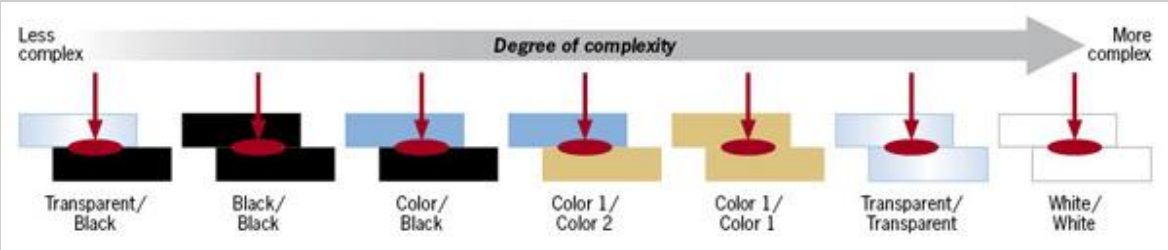
Custom processing

Laser welding

Features

- ✓ Ideal for sealing
- ✓ Ideal with polymers
- ✓ Complex geometries welding
- ✓ Small heat affected zone
- ✓ Aesthetic welding

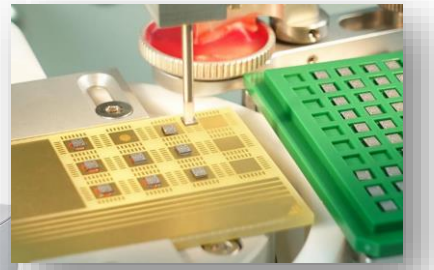


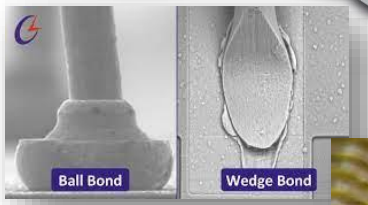


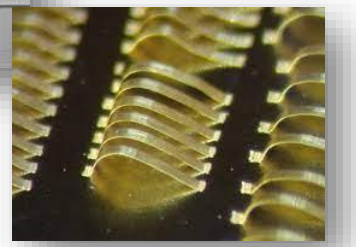
PCB and smart boards assembly

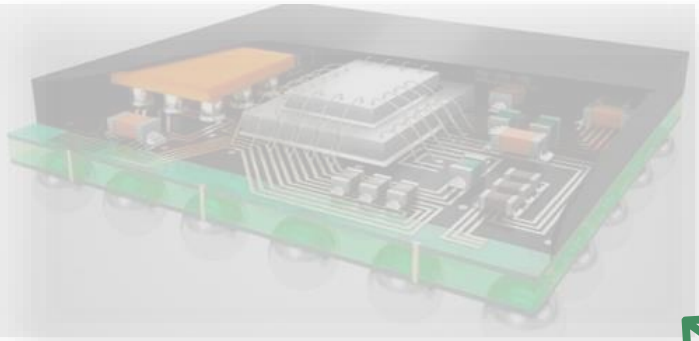
Wire bonder/Die bonder

Wedge/ball/ribbon bonding





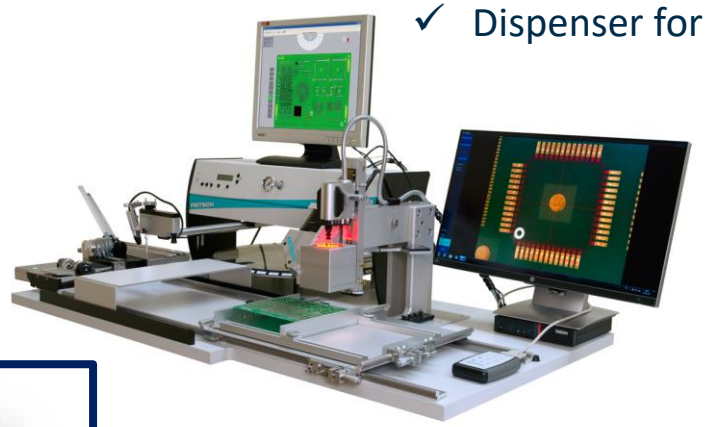




PCB and smart boards assembly

Pick and place

- ✓ Micrometric alignment
- ✓ Camera
- ✓ Dispenser for solder paste

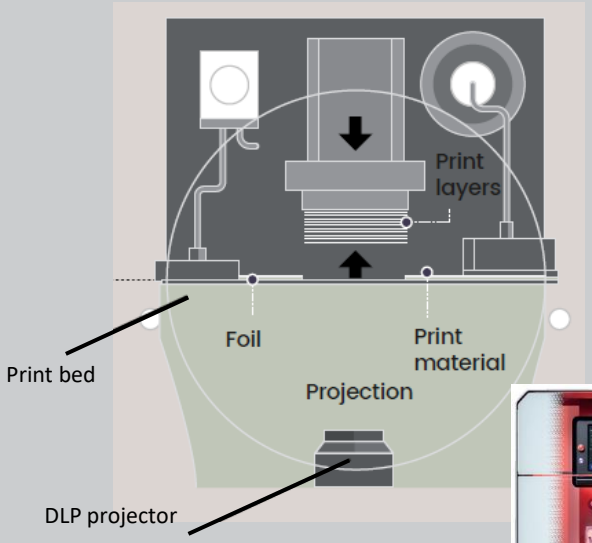


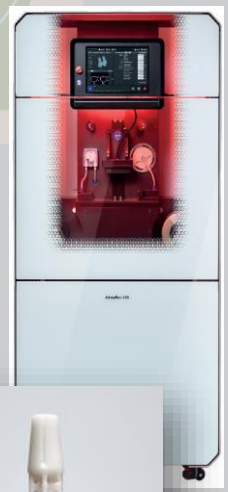
Reflow oven

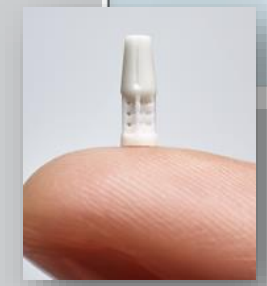
- ✓ IR oven
- ✓ Programmable soldering process

Additive manufacturing for packaging

Ceramic printing



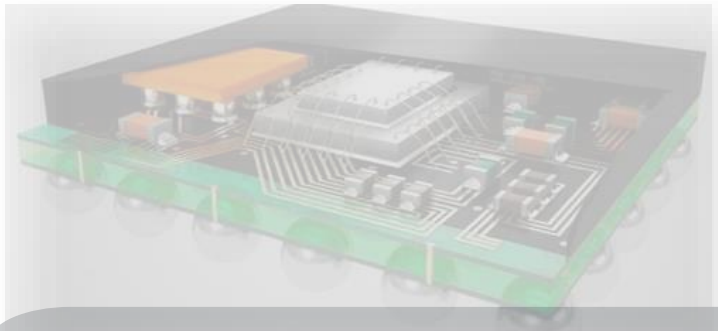




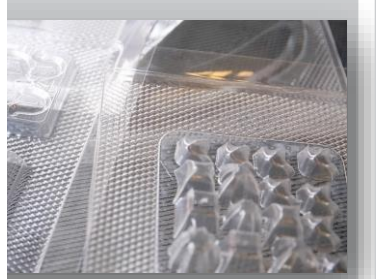
Features

- ✓ Custom or commercial material (alumina, zirconia, fused silica)
- ✓ Open platform

Additive manufacturing and Thermoforming



Thermoforming



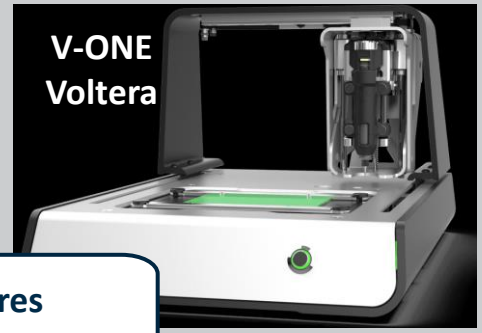
Electronics printing

Dragonfly NanoDimension

Features

3D print circuits in one step

- ✓ substrate
- ✓ conductive traces
- ✓ passive components



V-ONE Voltera

Features

- ✓ Quick PCB prototypes
- ✓ Drill and soldering

Multi-purpose platform for automated packaging

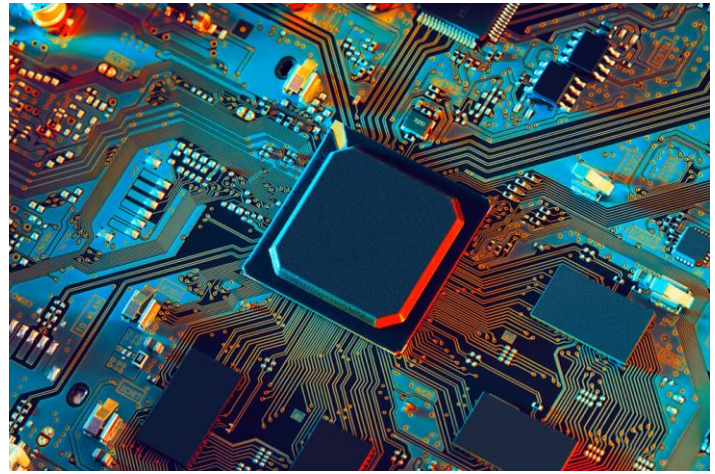
Laser etching

Laser welding

positioning

welding

Robot station

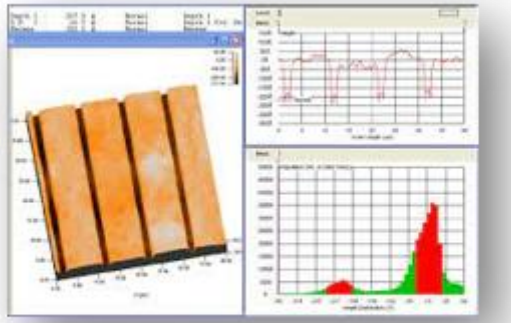


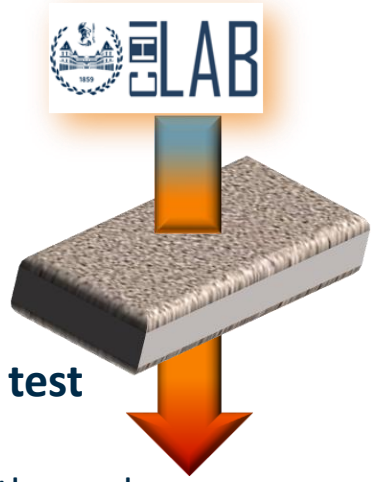
Testing facilities

Multiphysics simulation

Thermal, electrical, morphological characterization

Morphological characterization





Thermal conductivity test machine

Eterogeneous materials thermal transmission coefficient acquisition

Climatic chamber

Electrical and functional tests in simulated operating environment

National / Regional Research funds

PNRR funded running project

infrastructure for ENergy TRANsition and Circular Economy (iEntrance@ENL) (75 M€**)**
Provide the scientific community with access to micro- and nano- technology services

- CNR (IMM, ISM, NANO, ISMN, IMEM, IPCB, STEMS)
- **Politecnico di Torino (**14M€**)**
- Università Sapienza di Roma
- INRIM (Italy's National Metrology Institute)
- Università degli Studi Roma Tre
- Università di Bologna

PNRR funded infrastructure

Components and Systems for Energy Transition (COSyET) (40M€**)**

- IIT (Italian Institute of Technology) - Coordinator
- PiQuET (Piedmont Quantum Enabling Technologies
- **Chilab ITEM** (Interfacing Technlogies for Edge Microsystems)
- INRIM (Italy's National Metrology Institute

Industrial research project and experimental development of power devices. (€ 30 M€)

- Vishay Semiconductor Italiana S.p.A.
- Politecnico di Torino (DISAT)

iEntrance@ENL is a National Infrastrucure

INTERFACING TECHNOLOGIES FOR EDGE MICROSYSTEMS (**ITEM**)

Vision

Create a **meeting point** between research **labs and industries** to optimize and finalize **microsystems** prototypes fabrication exploiting **enabling technologies**

Mission

Our mission is to **study and develop materials** and **processes** by **interfacing** different **technologies** in order to encapsulate and dialogue **edge microsystems**

Remarks and Conclusions

1. **The microelectronics is approaching a new era,** and we are working to promote the innovation through **lectures**, **researches** and **technological transfer**
2. The Chilab-ITEM laboratory is in the process of installing new equipment dedicated to the manufacturing of interfaces and packaging
3. **We are dealing with the main companies**, based on their role in the microelectronics supply chain, we are mapping them across Italian regions
4. Detailed mapping activities will allow to build **matrices and networks of relations among companies within the value chain**, and to **inform policy actions**
5. The **extension of the supply chain** will allow to focus on **strategic stakeholders localized abroad**, providing important insights on possible incentives to FDI in our country

Microelectronics value chain

research in Turin

quantum technologies

micro- and nano manufacturing

energy transition

green energy

power electronics

advanced manufacturing

interfacing technologies

Thank you
for your kind attention

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di Torino

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