

# DEVELOPMENT OF THE CHIPS JU PARTNERSHIP OR How KDT JU BECOMES CHIPS JU?

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Torino, 24 October 2023



EUROPEAN  
PARTNERSHIP



with thanks to the Commission for the slides

1

## ENTRY INTO FORCE, 21 SEPTEMBER 2023

SIGNATURES 13 SEPTEMBER, PUBLICATION 18 SEPTEMBER 2023



Roberta Metsola (European Parliament President)

José Manuel Albares Bueno (Council Presidency)

**Chips Act:**

<https://eur-lex.europa.eu/eli/reg/2023/1781/oj>

**Single Basic Act amendment:**

<https://eur-lex.europa.eu/eli/reg/2023/1782/oj>



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2

## The context: we are/were in a crisis... (2021)

1

### Severe shortage of semiconductor chips

In a context of...

- Accelerated digital transition
- Increased demand for semiconductors
- Concentration of production in Asia (Taiwan, Korea)

No single Member State can face these problems alone, need for:

- EU & international partnerships
- Public subsidies

2

### Security supply risk in the EU

Due to...

- Limited capabilities in manufacturing
- Insufficient expertise in manuf. at < 20 nm
- High entry fees / cost for new facilities
- Geopolitical tensions (e.g. South China Sea)

3

### Detrimental effect across industries

Leading-edge semiconductor technology is central to...

- Competitiveness
- Security, safety and data protection
- Energetic performance of digital systems

Minus 11 million cars produced globally and 23% drop in German car sales in 2021.

## DIGITAL DECADE TARGET

Doubling of demand by 2030

20% of world production in value by 2030

Emerging market opportunities: AI, edge computing, digital transformation

Opportunities

Technological change: miniaturisation reaches its limits

Challenges

# EUROPE NEEDS A CHIPS ACT!



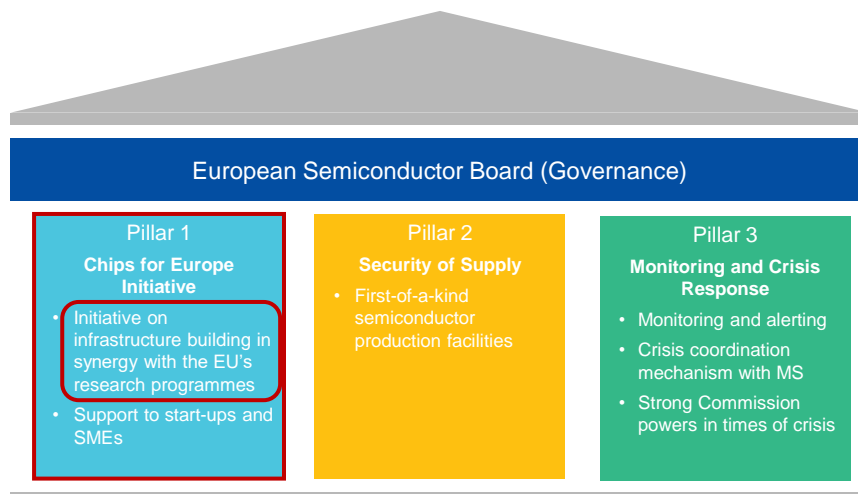
*Our aim is to jointly create a state-of-the-art European chip ecosystem, including production. We need to link together our world-class research, design and testing capacities. We need to coordinate EU and national investment along the value chain. This is not just a matter of our competitiveness. This is also a matter of tech sovereignty.*

Commission President Ursula von der Leyen, State of the Union speech,  
15 September 2021

Europe's objectives are:

- To **strengthen its research and technology** leadership
- To **build and reinforce its own capacity** to innovate in the design, manufacturing and packaging of advanced chips
- To put in place an adequate **framework to increase** substantially **its production** capacity by 2030
- To **address** the acute **skills shortage**
- To **develop** an in-depth **understanding** of the global **semiconductor supply chains**

## THE 3 PILLARS



Good to know  
but not in Chips JU

## CHIPS FUND



- **European Innovation Council** of Horizon Europe - promotes breakthrough innovation
- **EIC Accelerator**: support startups and SMEs to bridge the financing gap between R&D and market take-up
- Funding in the form of grants, equity and blended financing
- Thematic funding for semiconductor start-ups: **EU EUR 300 million** → ~EUR 900 million with partners



- **InvestEU** - Debt and equity programme to mobilise private and public investments in key areas through EU guarantees
- Implemented in partnership with EIB, EIF, financial institutions and promotional banks
- Funding available in the form of equity and debt products for R&I and production
- Thematic funding for semiconductor SMEs and scale-ups: **EU EUR 125 million** → ~EUR 1.25 billion with partners



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7

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## PILLAR 2: SECURITY OF SUPPLY

Framework to facilitate implementation of projects that **contribute to security of supply and strengthen resilience of semiconductor ecosystem** in the Union

### Label with benefit for companies:



**Beneficial treatment** of administrative applications



**Priority access to pilot lines** set up under the Initiative



Clear guidance how to demonstrate being **“first-of-a-kind”** in the Union

### In return:



Compliance with requirements to ensure security of supply and resilience



Investment in innovation to the benefit of the Union's ecosystem



Contributing through priority rated orders in a crisis



No additional burden through parallelism of State aid and labelling:  
Substantive synergies between the two processes



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8

## PILLAR 2: SELECTED INVESTMENT ANNOUNCEMENTS

 <b>BOSCH</b>	EUR 400 million, Dresden, Reutlingen (DE), Penang (MA), expanding wafer fabs
	USD 3.4+ billion, incl Agrate (IT), first industrialization line of new 300mm wafer fab
	EUR 300+ million, Bernin (FR), new fabrication facility for silicon carbide wafers
	EUR 30 billion, Magdeburg (DE), two fabs
	EUR 400 million, Vantaa (FI), wafer fab for 200 mm silicon wafer production
 	EUR 5.7 billion, Crolles (FR), jointly operated 300-mm manufacturing facility for FD-SOI-based technologies
	USD 300 million, Rožnov (CZ), expansion of SiC fab
	EUR 10 billion, Dresden (DE), JV between TSMC, Bosch, Infineon, NXP
	EUR ??? million, Barcelona (ES), design centre for “next generation semiconductor devices”
	EUR 5 billion, Dresden (DE), new factory for 300-millimeter analog/mixed-signal and power semiconductors
 	USD 3 billion, Ensldorf (DE), joint 200-millimetre SiC fab and R&D centre



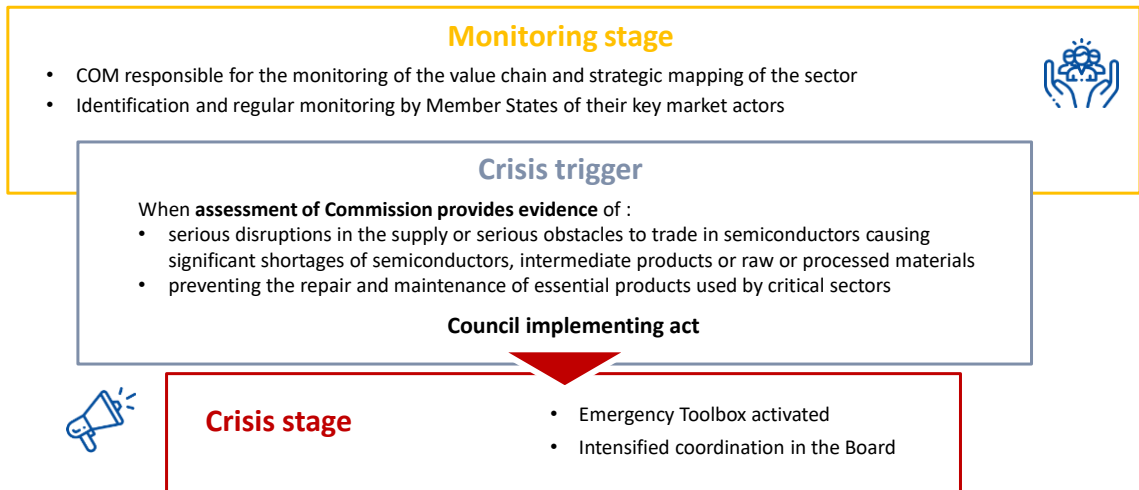
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9

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## PILLAR 3: MONITORING AND CRISIS RESPONSE



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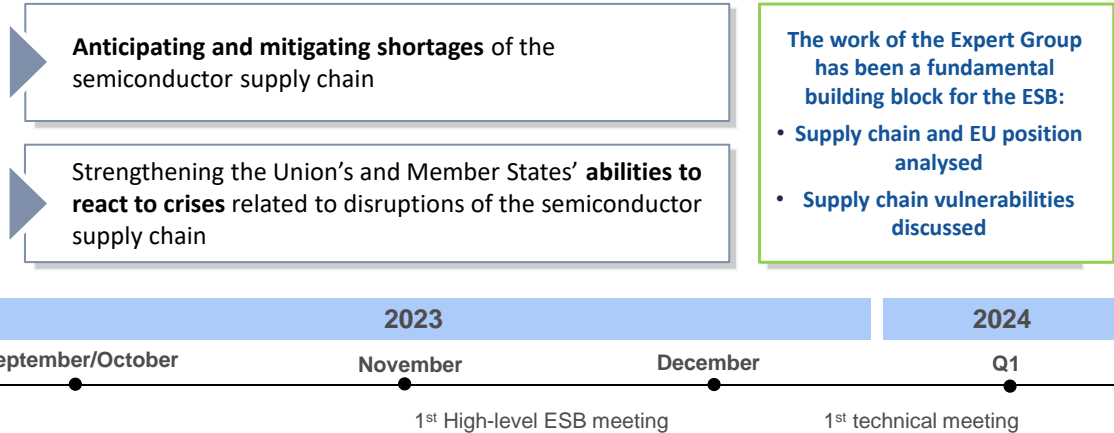
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10

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## EUROPEAN SEMICONDUCTOR BOARD

- The European Semiconductor Board (ESB) as coordination body:



11



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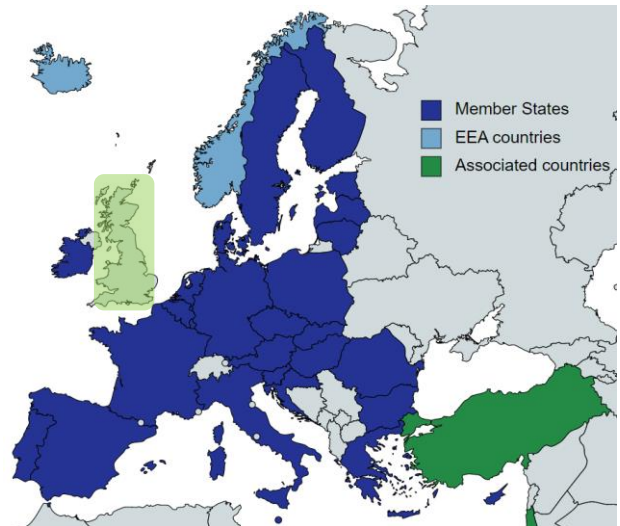


11

## FROM KDT JU TO CHIPS JU

- KDT General Objectives**
  - Reinforce EU strategic autonomy in electronic components and systems
  - Establish EU scientific excellence and innovation leadership
  - Ensure that components and systems technologies address Europe's societal and environmental challenges
- From KDT to Chips JU**
  - Pilot lines
  - Design platform
  - Competence centers
  - Quantum chips technology

Digital Europe Programme in addition to Horizon Europe  
Tweaks in governance to deal with strategic Initiative and increased funds
- Increased budget**  
From EUR 1.8 billion to **EUR 4.175 billion**

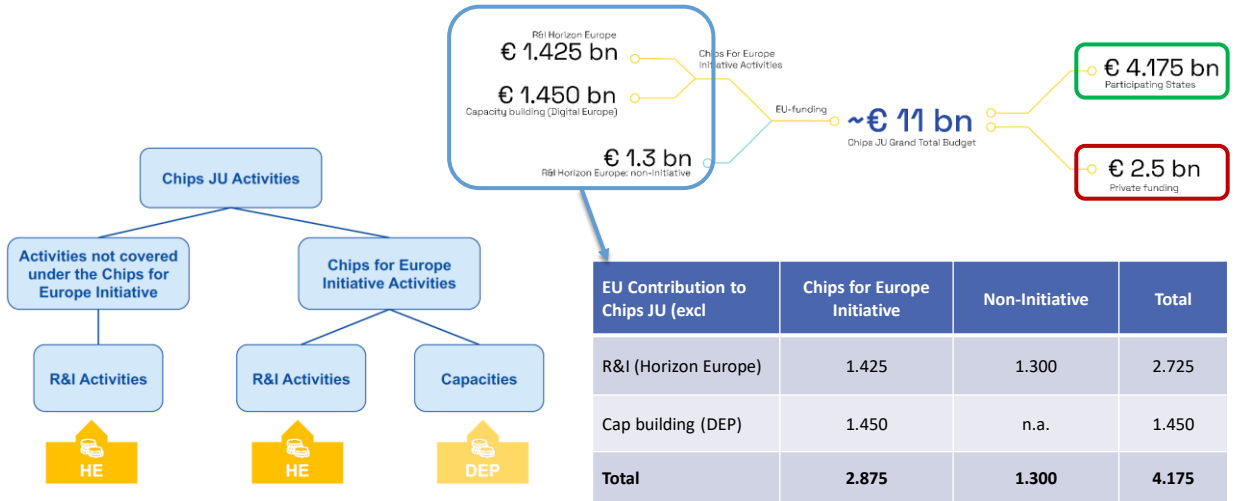


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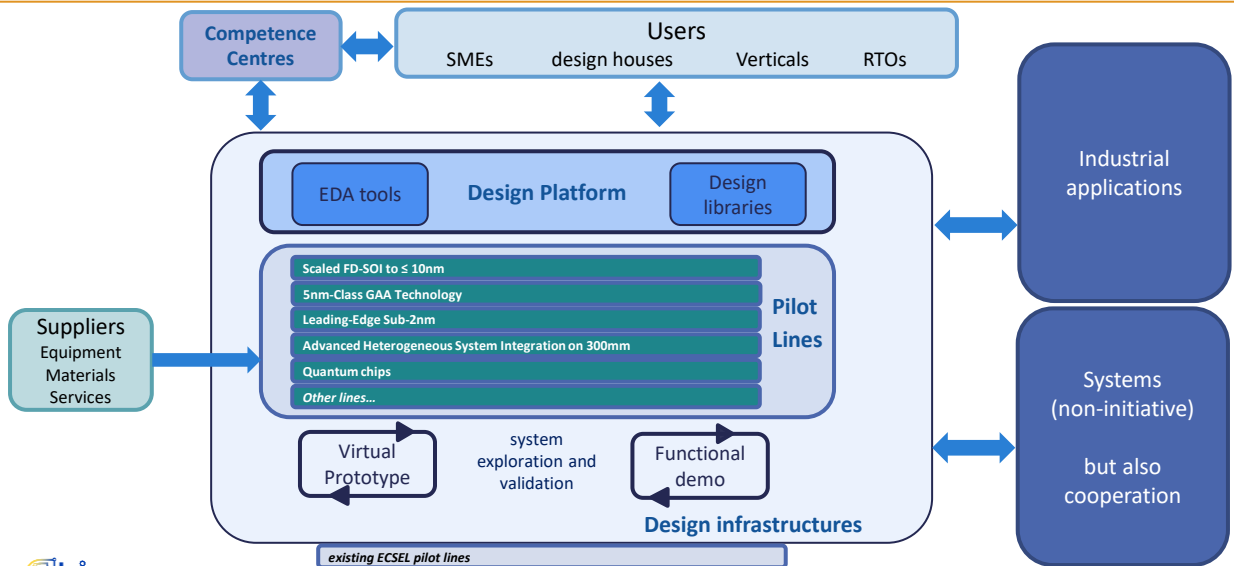


12

# CHIPS JU



## CHIPS JU: THE INITIATIVE PART



## SERVICES PROVIDED BY THE DESIGN PLATFORM



**Ambition:** to provide start-ups, SMEs and other users a design environment similar to what is expected at larger companies through the aggregation of demand

## COMPETENCE CENTRES

- Have specialised areas of expertise in certain technology, domain, or activities (**specialisation**)
- Facilitate effective use of capacities and facilities, including access to **design platform** and **pilot lines**
- Support interested stakeholders in developing semiconductor solutions (**technology transfer**)
- Address **skills shortage** by offering (access to) **training** on semiconductors, including workforce upskilling and reskilling
- Match user needs with available expertise in network of competence centres and act as **access point to the network**
- **Promote Chips Fund** and facilitate access to venture capital
- **Awareness raising, promoting services, promoting success stories**



# TIMELINE

## Pilot Lines

- End 2023 (Nov/Dec): First call
- Q2 2024: First selection of pilot lines the PAB
- 2024 : further calls for proposals for pilot lines with selection in 2025

## Design Platform

- Call in Q1 2024
- Q2 2024: selection of project

## Competence Centres

- 2024 Q1: Member States to designate candidate competence centres
- 2024 Q2: restricted call for designated candidate competence centres
- 2025 Q1: second restricted call for the remaining Member States

## Non initiative part

- 2024 Q1: Launch of calls 2024 (RIA & IA)
- 2024 Q4: selection of projects

# CALLS 2024: NON INITIATIVE

WP2024 by end of year containing:

- RIA and IA general calls
- **Focus topics (not yet decided!)**
  1. Packaging and 3D Heterogeneous Integration applied to RF/mmWave Transceivers with compatibility to serve 6G
  2. Sustainable and greener manufacturing
  3. Service Oriented Framework for the Software Defined Vehicle of the future
  4. High Performance RISC-V Automotive Processors supporting SDV
  5. AI-assisted methods and tools for ECS engineering efficiency
- Other? (eg International cooperation)

## IN ADDITION: INTERNATIONAL COOPERATION

### Strategy outlined in Communication

- Proactively manage interdependencies with the rest of the world with a twofold objective:
  - (i) to ensure reliable global marketplace for European products, and
  - (ii) to ensure security of supply, including in crisis situations

### Need for balanced semiconductor partnerships with like-minded countries

- Possible elements of partnerships: better visibility of potential shocks by regularly sharing information on mitigating upcoming shortages and effective early warning mechanisms; international standardisation; workforce development; coordination on export controls; research cooperation

**Chips JU will implement part of the actions**

COM(2022) 45, 8 February 2022



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19

## WANT TO KNOW MORE ?



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20

## QUESTIONS

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