Metrology challenges for the semiconductor industry

An ASML Perspective

Wim Coene and Lorenzo Tripodi
ASML-Research, Metrology Department

July 8th 2022
Veldhoven, The Netherlands

wim.coene@asml.com
lorenzo.tripodi@asml.com

EURAMET – Meeting “Open Consultation on Semiconductor Metrology”
July 8th 2022

Outline

- Introducing ASML
- Holistic Patterning Triangle and Overlay Metrology
- From Overlay metrology to EPE(*) metrology
- Landscape of Technologies for Semicon Metrology

EPE(*) = edge placement error

Introducing ASML

All major chipmakers use ASML's technology

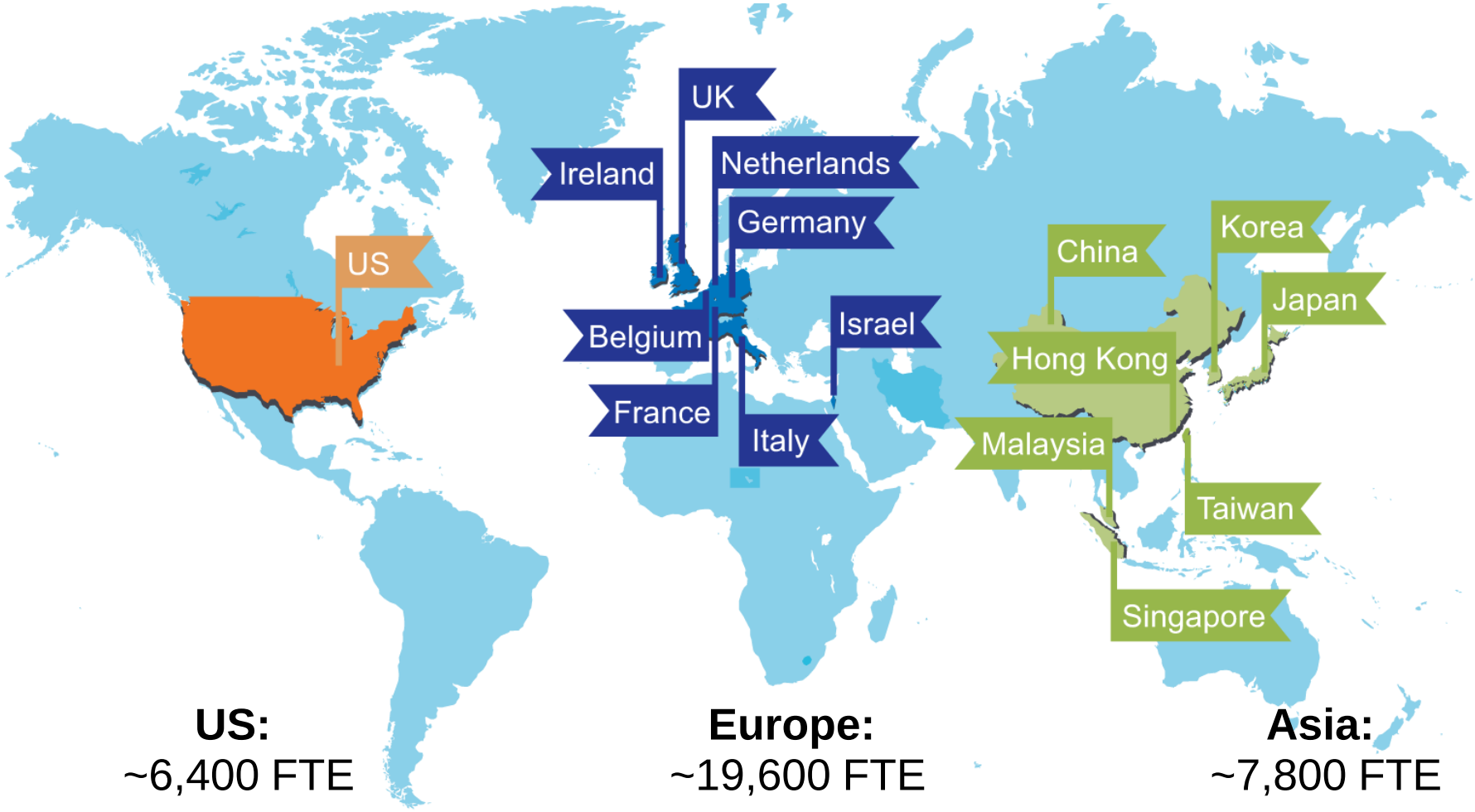
Europe's biggest tech company by market cap

Annual R&D budget of €2.5bn

SAMSUNG
SMIC
tsmc
XMC
intel
SONY
Micron
华虹集团 HUAHONG GROUP
SK hynix
KIOXIA

A global presence with ~34,000 employees (Q1 2022)

Offices in over 60 cities in 16 locations worldwide



US:
~6,400 FTE

Europe:
~19,600 FTE

- Netherlands: ~17,900
- ASML Berlin: ~1,300
- Europe other: ~400

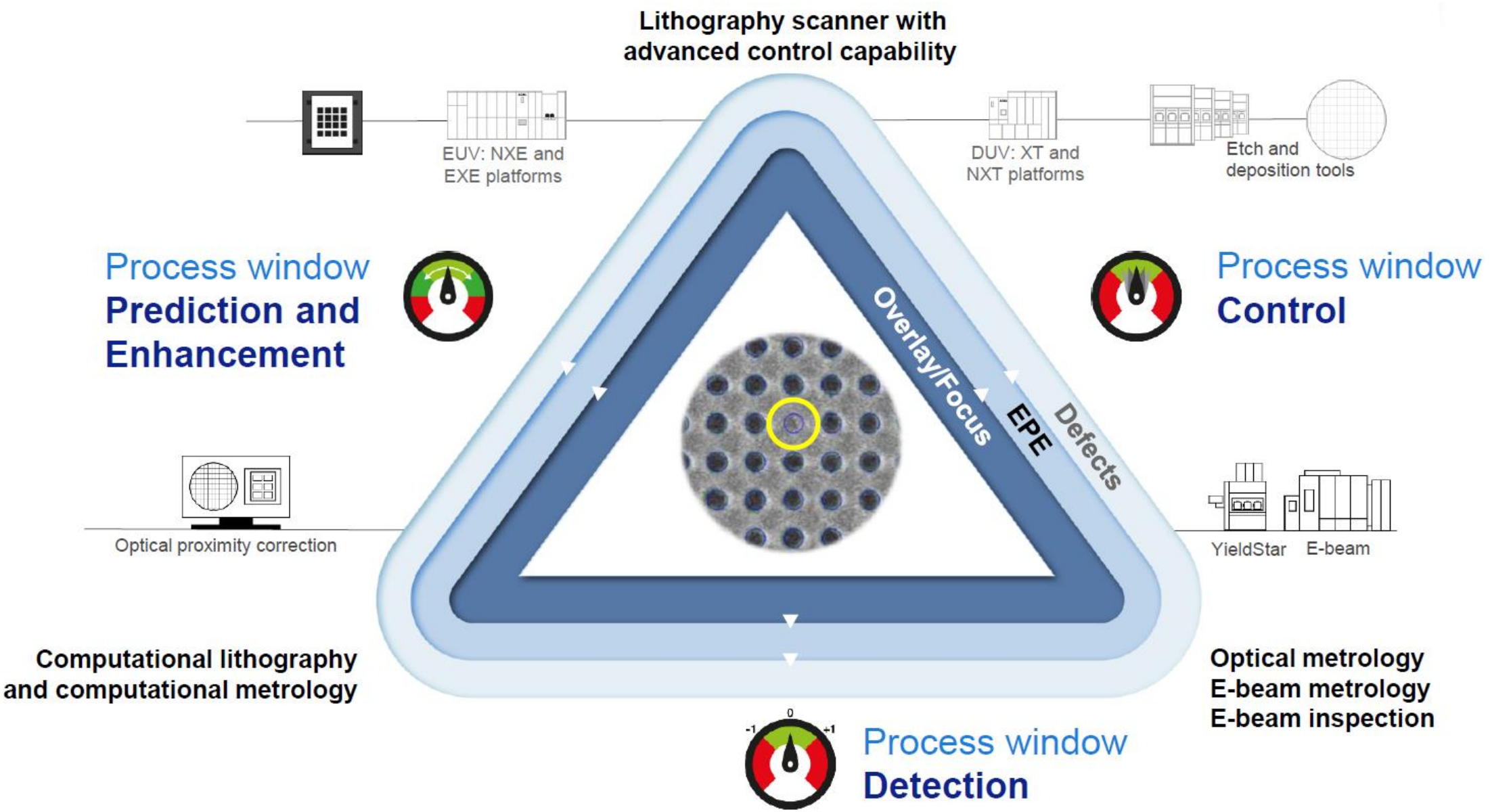
Asia:
~7,800 FTE

Outline

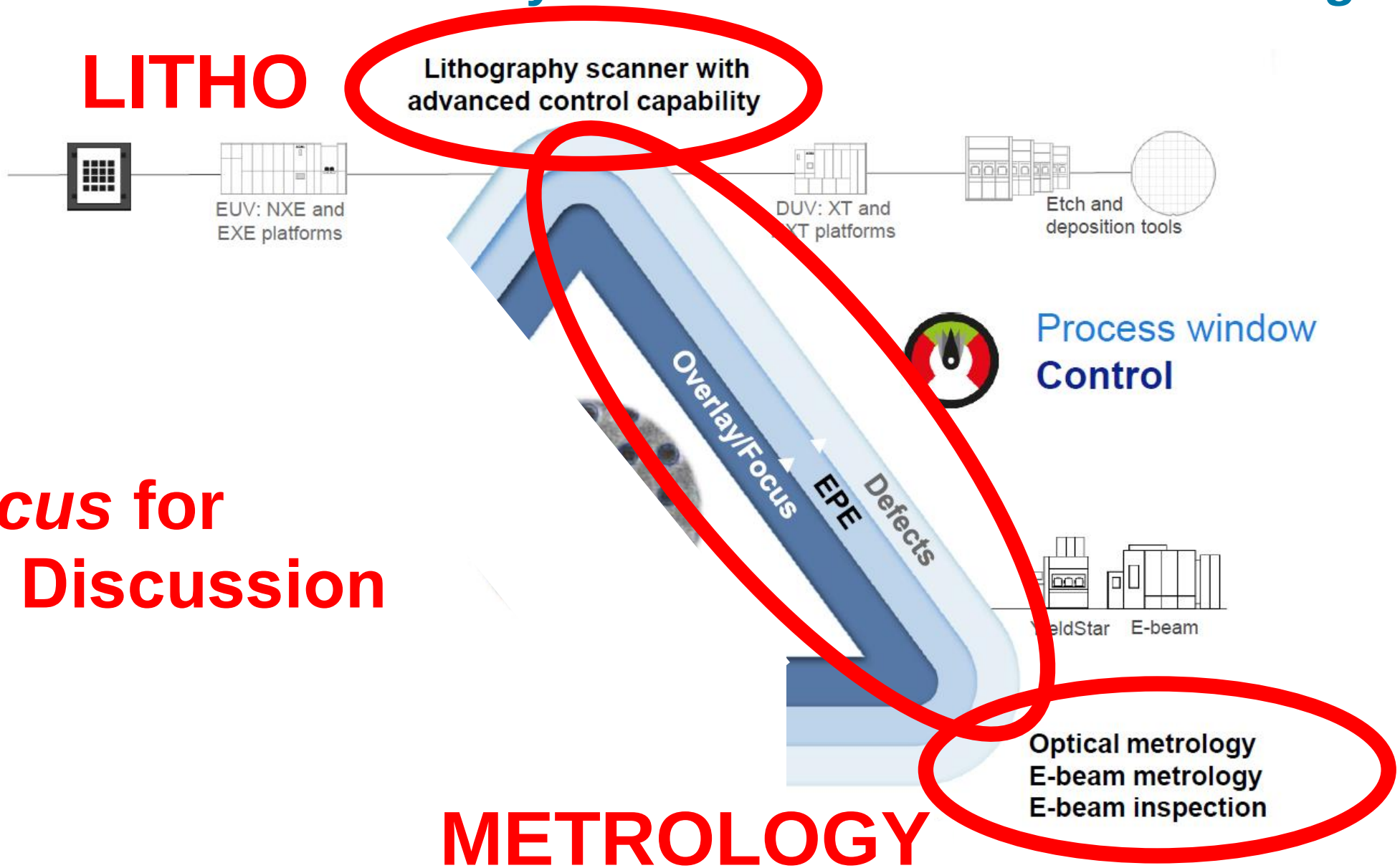
- Introducing ASML
- **Holistic Patterning Triangle and Overlay Metrology**
- From Overlay metrology to EPE(*) metrology
- Landscape of Technologies for Semicon Metrology

EPE(*) = edge placement error

Metrology @ ASML : one of the 3 key-elements of *Holistic Patterning*



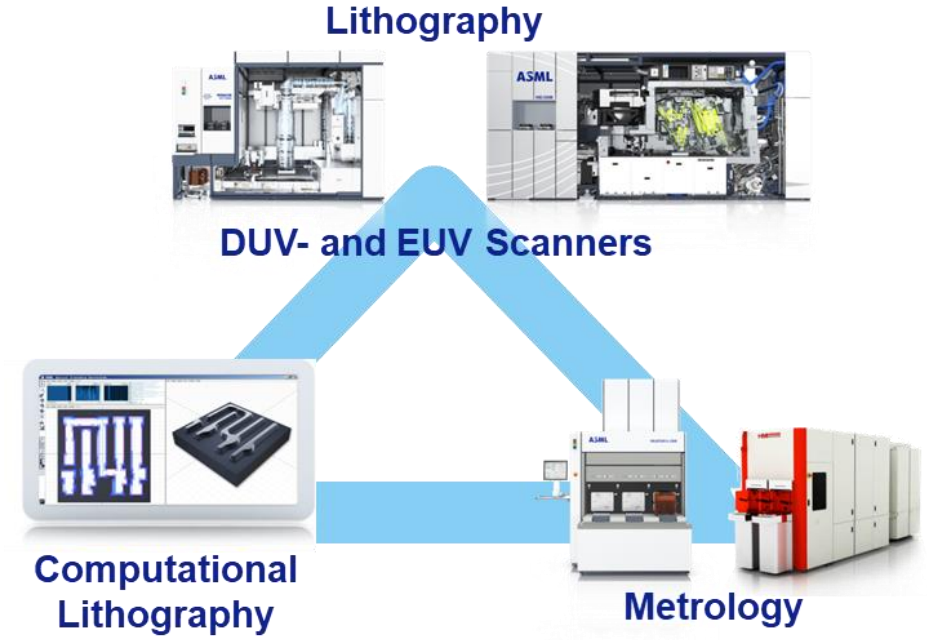
Metrology @ ASML : one of the 3 key-elements of *Holistic Patterning*



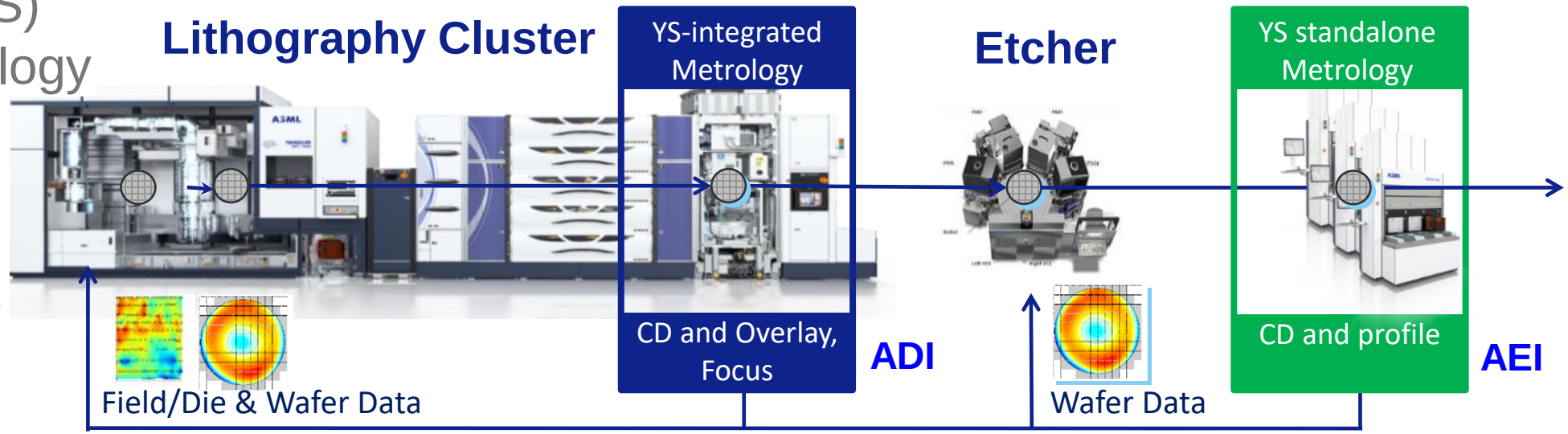
***Focus* for Today's Discussion**

Metrology @ ASML : one of the 3 key-elements of *Holistic Patterning*

Holistic Lithography and Patterning



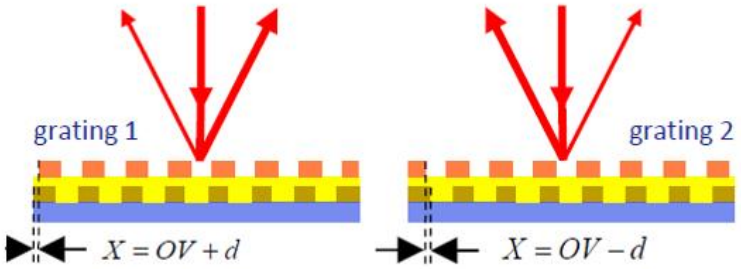
YieldStar (YS) Wafer Metrology



ADI = after-development inspection

AEI = after-etch inspection

Current Optical METROLOGY @ ASML : mainly diffraction-based overlay metrology (DBO for ADI)

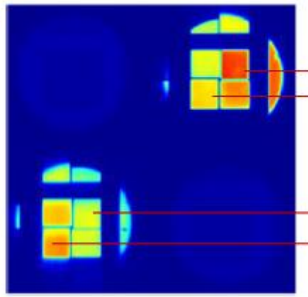


$$A^+ = K(OV + d) \qquad A^- = K(OV - d)$$

K is overlay sensitivity
A is asymmetry (delta Intensity)
d is grating bias

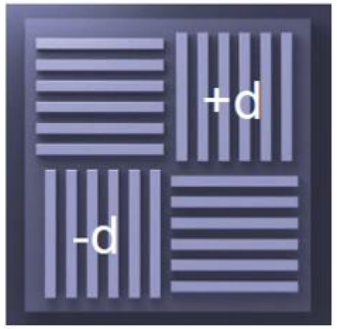
Measured OV: $$OV = d \times \frac{A^+ + A^-}{A^+ - A^-}$$

YieldStar Image of µDBO target on the wafer



$$A^+ = I_{+d}^{(+1st)} - I_{+d}^{(-1st)}$$

$$A^- = I_{-d}^{(+1st)} - I_{-d}^{(-1st)}$$



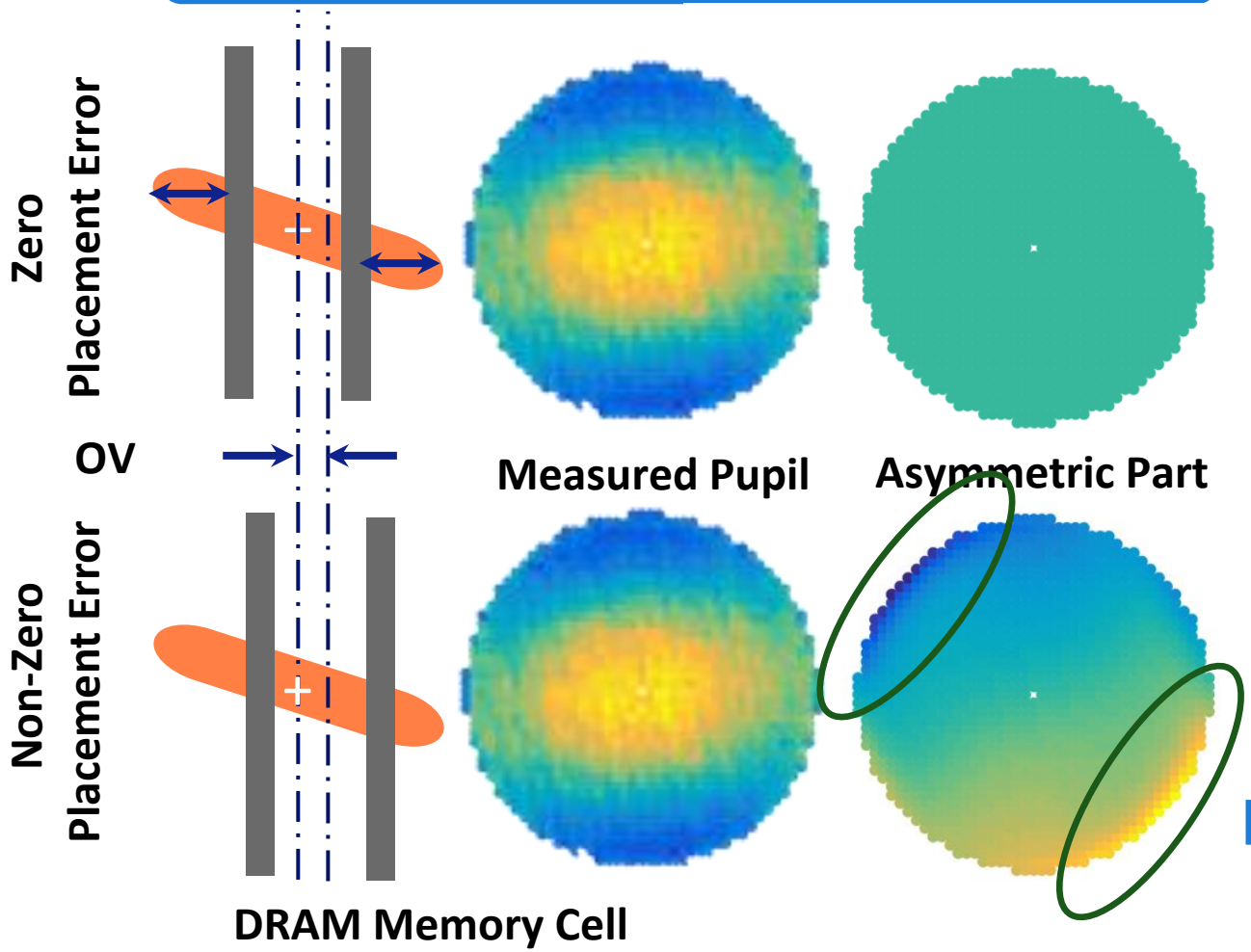
µDBO target on the wafer

From: https://www.3d-metrology-workshop.eu/images/presentations_2018/6_Paul_Hinnen.pdf

In-Device Metrology (IDM) Overlay: Concept

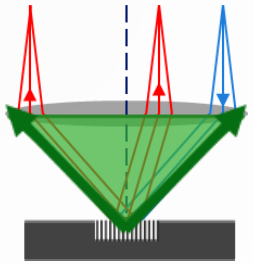
0th-Order Pupil Asymmetry signals are a measure for Overlay

Overlay Principle

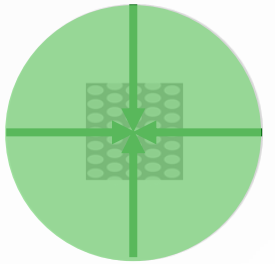


Overlay Metrology

High 0.95 NA Continuous Angles



All Azimuthal Directions



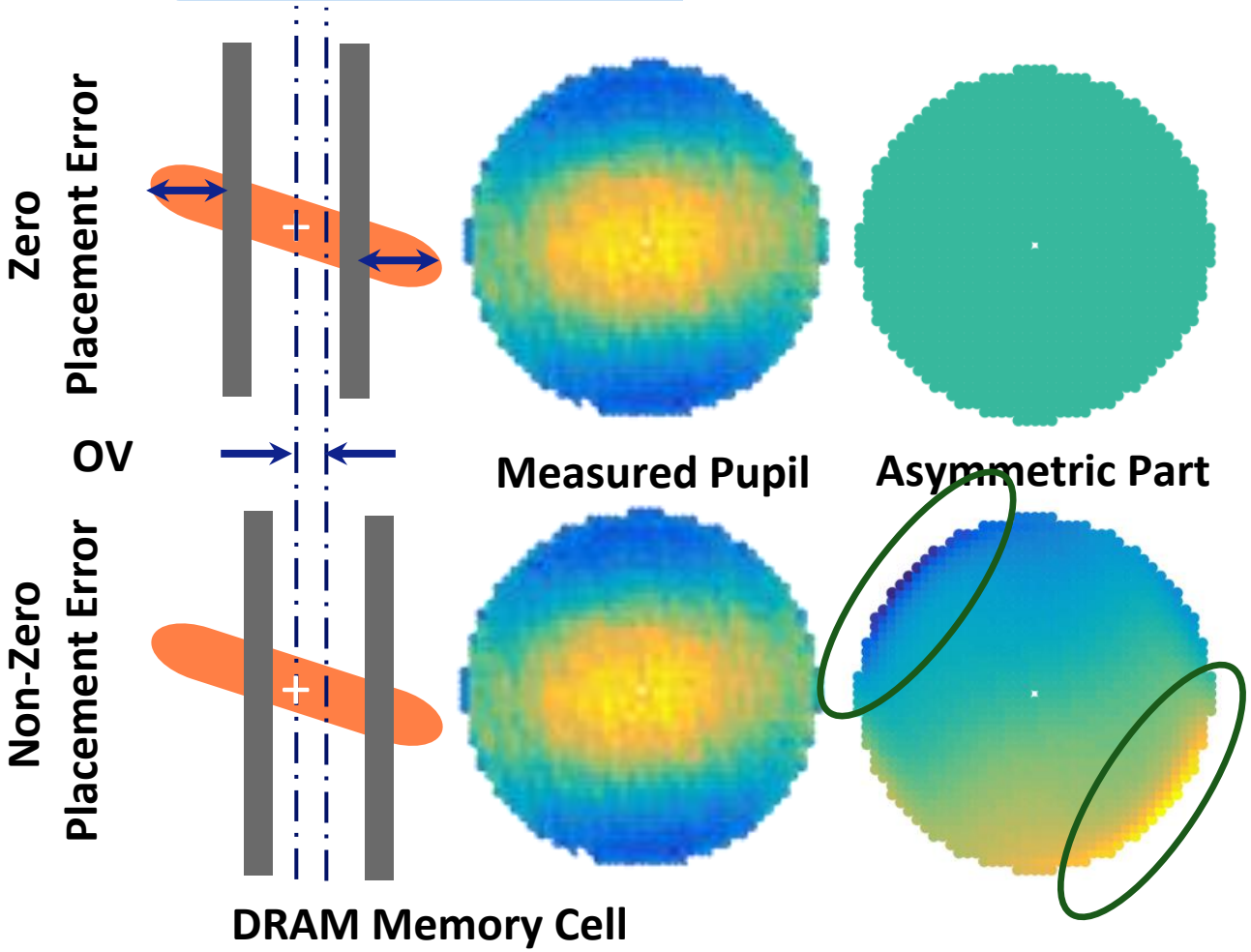
Overlay asymmetry signal fully captured with high NA

Overlay signal typically at the edge of the pupil

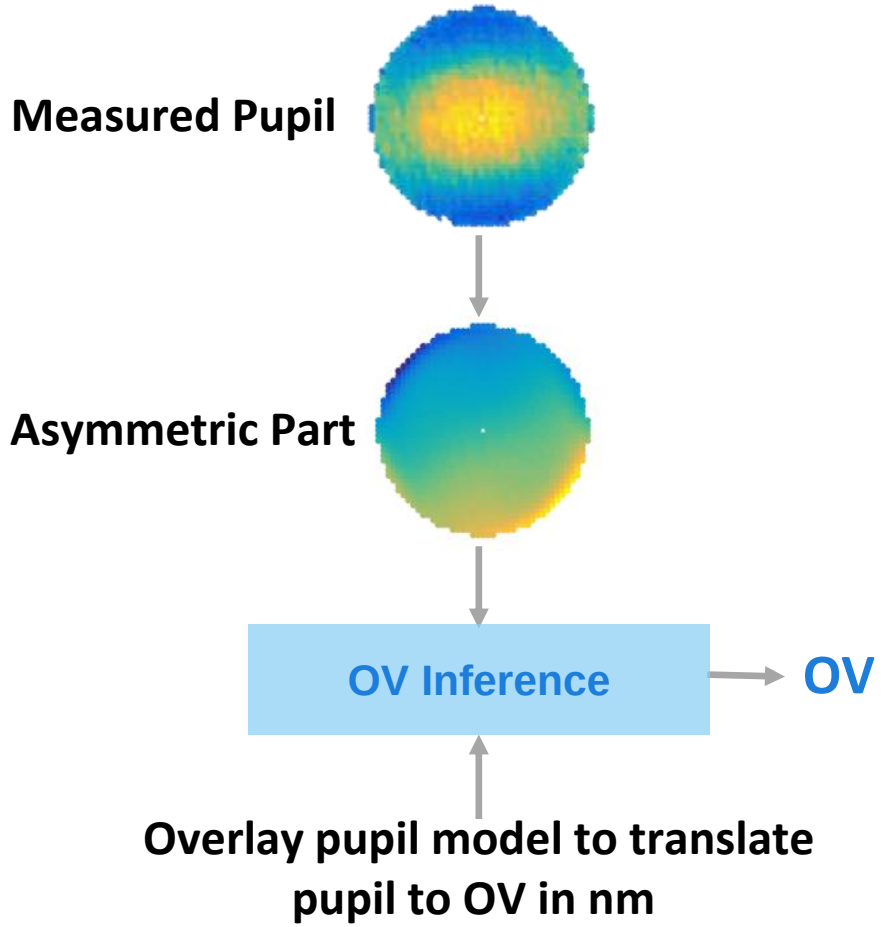
In-Device Metrology (IDM) Overlay: Concept

0th-Order Pupil Asymmetry signals are a measure for Overlay

Overlay Principle



Overlay Metrology



Outline

- Introducing ASML
- Holistic Patterning Triangle and Overlay Metrology
- **From Overlay metrology to EPE(*) metrology**
- Landscape of Technologies for Semicon Metrology

EPE(*) = edge placement error

From overlay-metrology towards EPE(*)-metrology

Multiple patterning DUV + EUV

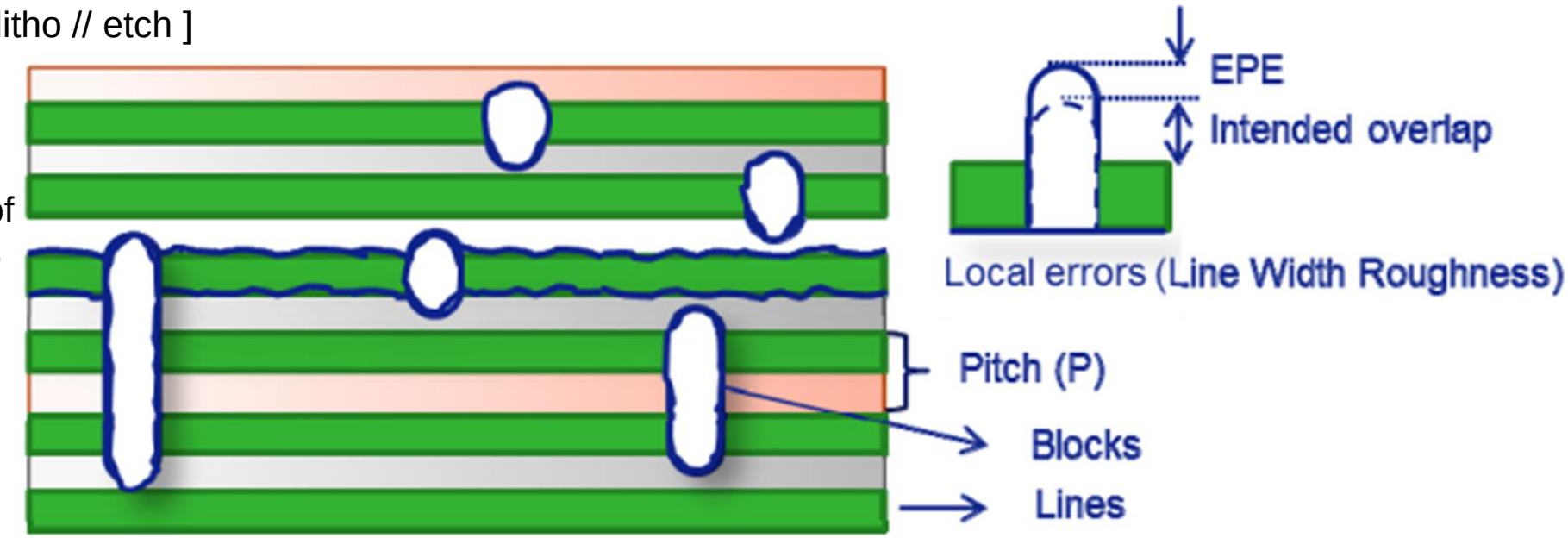
- 1D-grating with DUV (193nm) + Self-Aligned-Quadruple-Patterning (SAQP)
  - Multiple exposures : [litho // etch]^n
- Cut-pattern of 2D block-structure with EUV (13.5nm)
  - Single exposure : [litho // etch]

- EPE is the better proxy for *yield*
- EPE results from a combination of *global* (CD, OVL) and *local* errors (*LWR, LER*)

$$EPE_{max} = \frac{HalfRange_{OPC}}{2} + \frac{3\sigma_{PBA}}{2} + \frac{6\sigma_{LWR}}{\sqrt{2}} + \sqrt{(3\sigma_{overlay})^2 + (\frac{3\sigma_{CDU}}{2})^2}$$

with $\sigma_{LWR} = \sqrt{\sigma^2_{LWR,line} + \sigma^2_{LWR,block}}$

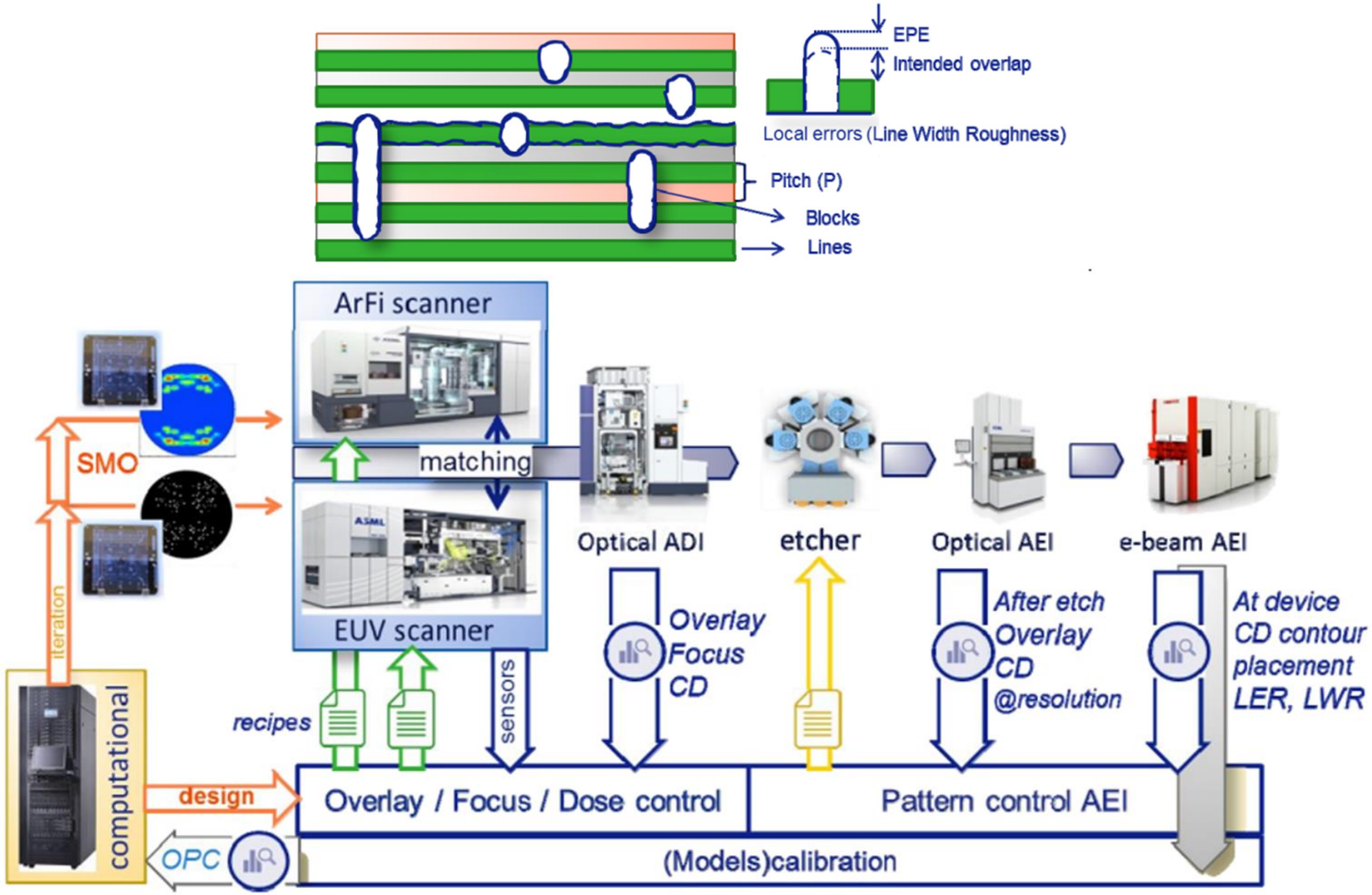
and $\sigma_{CDU} = \sqrt{\sigma^2_{CDU,line} + \sigma^2_{CDU,block}}$



EPE(*) = edge placement error

Jan Mulkens et al, Metrology, Inspection, and Process Control for Microlithography XXXII, Proc. of SPIE Vol. 10585, 105851L

From overlay-metrology towards EPE-metrology (2)



Jan Mulkens et al, Metrology, Inspection, and Process Control for Microlithography XXXII, Proc. of SPIE Vol. 10585, 105851L

Outline

- Introducing ASML
- Holistic Patterning Triangle and Overlay Metrology
- From Overlay metrology to EPE(*) metrology
- **Landscape of Technologies for Semicon Metrology**

EPE(*) = edge placement error

Semi-Con METROLOGY: Landscape of Diverse Needs & Technologies

NEEDS

- Overlay Metrology
- EPE-Metrology
- Defect Inspection
- Profilometry

KPI's

- Throughput
- Reproducibility
- Accuracy
- Resolution
- Ease-of-Use (simple recipes)

Litho - Scanner

- EUV High-NA 0.55
  - Reduced Depth-of-Focus (focus metrology)
- Multi-litho
  - ≥ double patterning
  - Combined lithography DUV + EUV

TECHNOLOGIES

OPTICAL METROLOGY

- Optics Design
- Sources
- Detectors
- Large Wavelength Range
- EUV/SXR Metrology

E-BEAM

- Metrology: single-beam
- Inspection: multi-beam

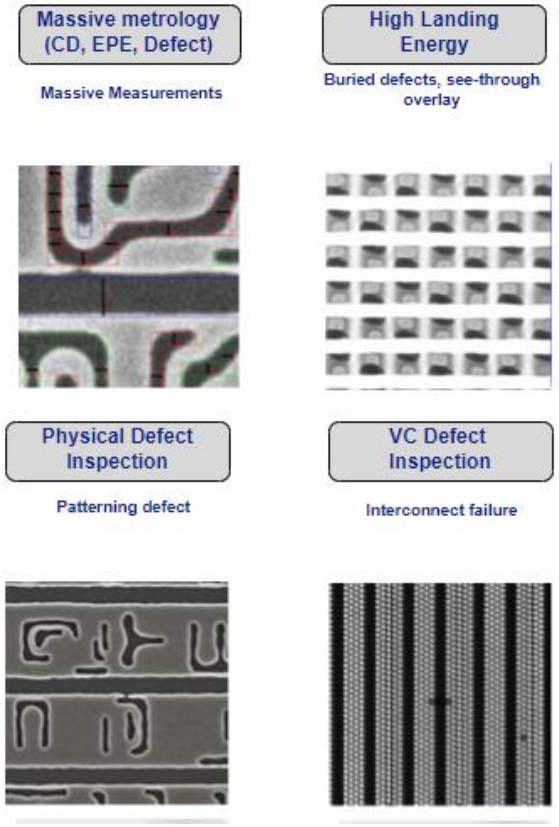
COMPUTATIONAL ASPECTS of OPTICAL METROLOGY

- Computational Imaging
- Aberration Correction
- Lensless Imaging
- Inverse Problems & Parameter Inference

SOME ACTIVITIES (ASML)

- YieldStar

- HMI – Single-beam/Multi-beam



Metrology Needs related to Future Trends in IC-Technology

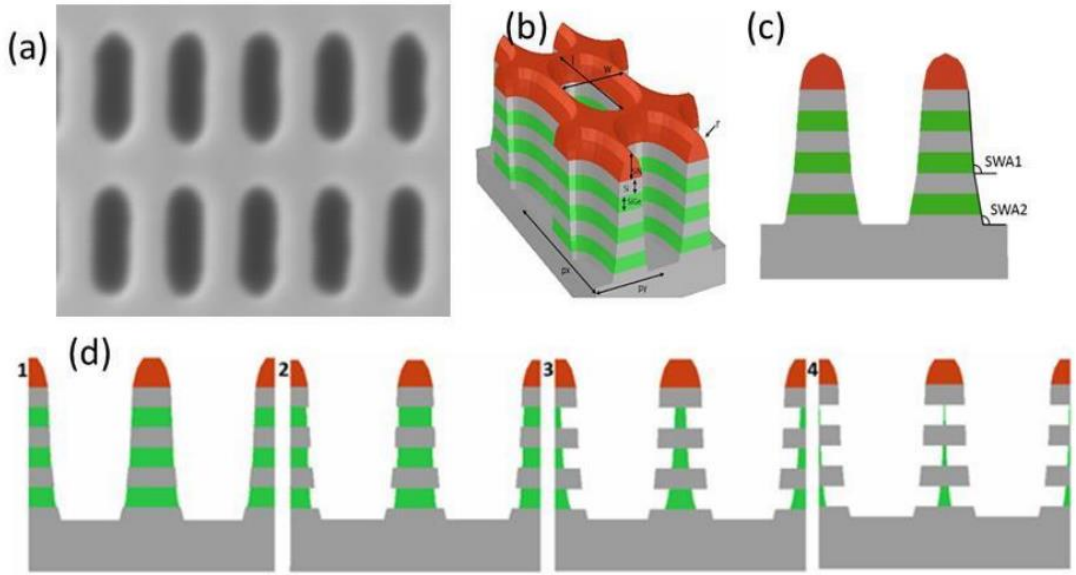


Figure 4. The NWTS and the selective etch of subsurface SiGe layers is shown. A top down view of the holes in the test structure is shown in (a). A section of the optical structure model used for scatterometry simulations is shown in (b). A cross-section along the narrow part of the hole structure is shown in (c). The selective etch of the SiGe subsurface layers is shown in (d). The structures shown in (d) represent a cross-sectional view of the optimized optical model for the selectively etched structures. The amount of selective etch is (1)3.4nm, (2)10.5nm, (3)18.9nm and (4)21.9nm from the sidewall. Figure adapted from Reference 16 with copyright AIP and used with the authors' permission.

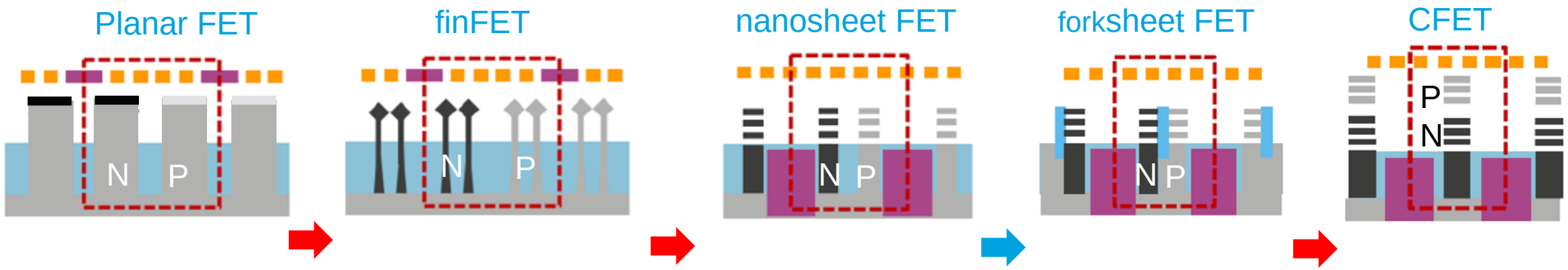
Separate challenges not covered by EPE

- Nanowire/Nanosheet Gate-all-around FETs with Si/SiGe/…/Si fins.
- Selective etch:
  Ge-recess is important KPI
- Ge-recess is not measured by EPE

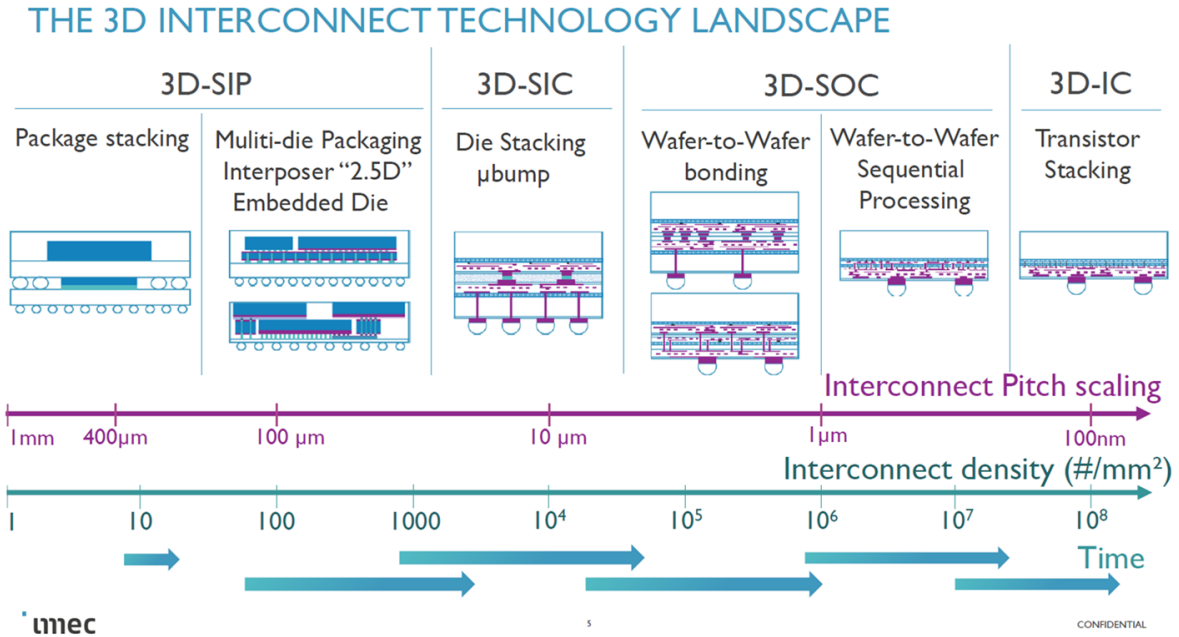
From: Alain C. Diebold, Nathaniel C. Cady, "Metrology for advanced transistor and memristor devices and materials," Proc. SPIE 11325, Metrology, Inspection, and Process Control for Microlithography XXXIV, 1132502 (2020).

Future Trends in IC-Technology (IMEC)

- transistor evolution according to IMEC



- 3D extension via Chip-to-Chip bonding (IMEC)



ASML