"Europe will not be made all at once, or according to a single plan. It will be built through concrete achievements which first create a de facto solidarity."
Robert Schuman

THE KDT JOINT UNDERTAKING. THE EUROPEAN PROGRAMME FOR RD&I IN ELECTRONIC COMPONENTS AND SYSTEMS.

OPEN CONSULTATION ON METROLOGY FOR SEMICONDUCTOR TECHNOLOGIES

Yves GIGASE
Head of Programmes
08 July 2022

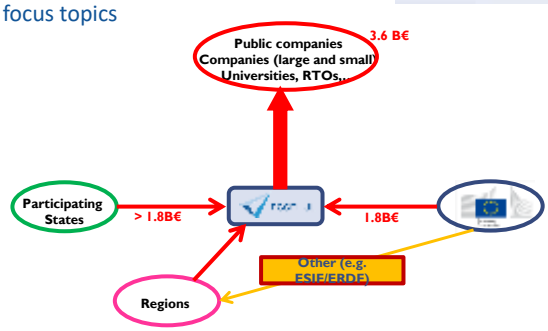
EUROPEAN PARTNERSHIP

1

1

KDT JU 2021-2027

- Third generation JU (start 30/11/2021), predecessor was ECSEL JU
- KDT JU = Key Digital Technology Joint Undertaking
- Tripartite: Commission - Participating states – Industry associations
- Associations: AENEAS, INSIDE, EPoSS
- Budget ambition : 7.2B€ funded by 1,8 B€ (EU)+1,8 B€ (national)
- Based on Horizon Europe
- **Bottom-up** programme with **top-down** focus topics
- "**Value chain**" approach
- **Pilot lines** (higher TRLs)
- **critical mass** approach
- focussed on **industrial leadership**
- **common agenda of** Europe's ECS

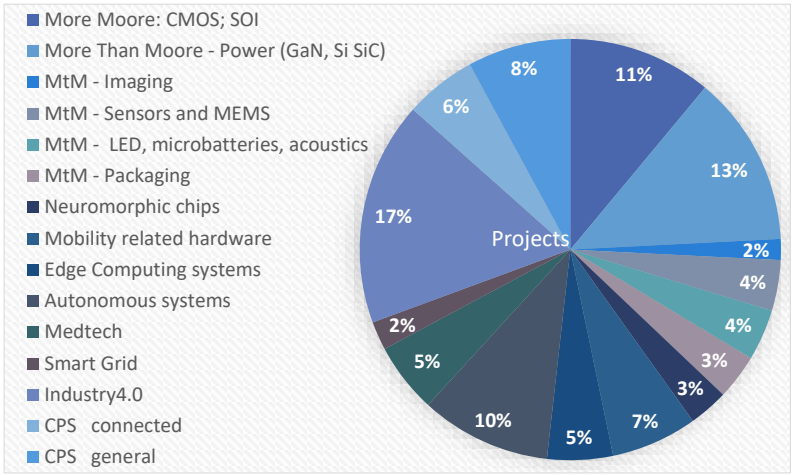


https://www.kdt-ju.europa.eu/

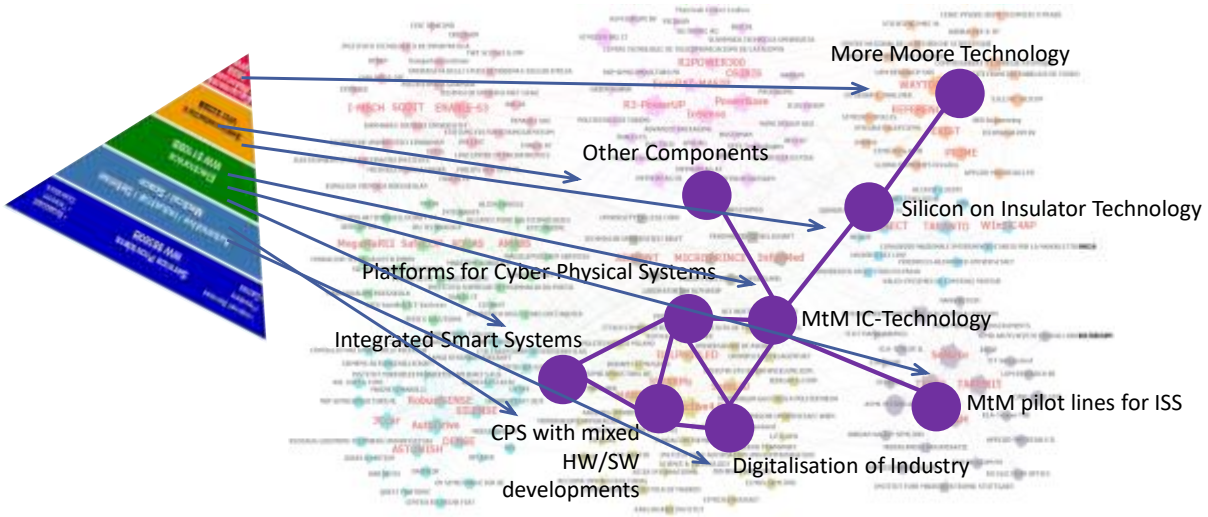
2

ECSEL JU 2014-2021

- 92 projects
- 3 220 beneficiaries
- 4 690 million Eur in total cost
- 2 280 million Eur in funding (EU+national)
- 408 500 persons-months
- 29 participating states



NETWORKS OF PARTNERS AND PROJECTS

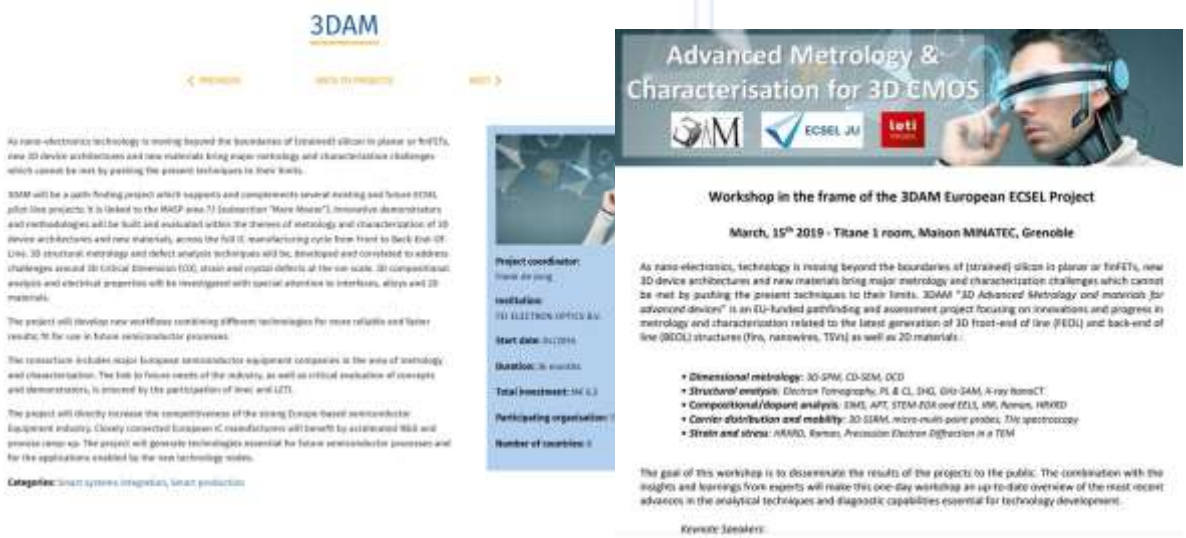


MORE MOORE PROJECTS

All with participation of PTB

5

3DAM



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MADEIN4

MADEIN4

Metrology Advances for Digitized Electronic Components and Systems (ECS) Industry 4.0

MADEin4

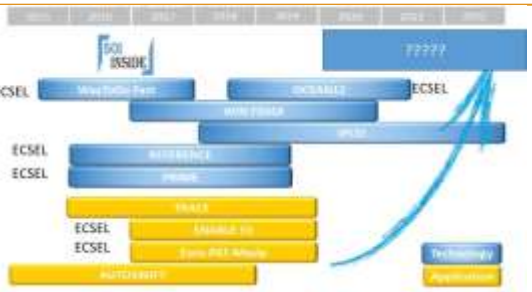
THE MADEIN4 PROJECT IMPROVES INDUSTRY 4.0 MANUFACTURING PRODUCTIVITY BY DEVELOPING

PILOT LINE PROJECTS AND PROJECT SUITES

More Moore

The projects contribute directly to the European Strategic Roadmap for Micro- and Nano-Electronics Systems

SOI



Power components

Description of projects on KDT website https://www.kdt-ju.europa.eu/

from ASML

MATQu

Q-COMPUTING

POWER2POWER

Example
Development and implementation of an ultra-precise wafer thinning process. Set up an appropriate metrology and data processing in this area.

YESVGAN

POWER ELECTRONICS

YES vGaN
Wide Band Gap Power at Silicon Cost

YESvGaN will establish a new class of vertical GaN power transistors which combines the performance benefits of vertical Wide Band Gap (WBG) transistors with the cost advantages of established silicon technology. These transistors can replace IGBTs and thus reduce power conversion losses in many price-sensitive applications ranging from power supplies in data centers to traction inverters for electric vehicles. YESvGaN covers the development of the required new technology all the way from wafer to application.

Possible electricity savings in the EU in 2030 by consequent implementation of YESvGaN vertical membrane GaN transistors in the target applications

PROGRESSUS

PROGRESSUS

HOME NEWS PROJECT CONSORTIUM PUBLICATIONS CONTACT

Highly Efficient and Trustworthy Electronics, Components and Systems for the Next Generation Energy Supply Infrastructure

Next Generation Smart Grid to reduce Greenhouse Gas Emissions and Grid Peak Power

The high-power requirements of ultra-fast charging stations give rise to special challenges when designing smart charging infrastructure. In support of Europe's 2030 climate targets, the EU-funded PROGRESSUS project aims to introduce a next-generation smart grid demonstrated by the application example of a smart charging infrastructure integrating seamlessly into current smart-grid architecture concepts. To do so, it will research new efficient high-power converters that support bidirectional power flow. New DC microgrid management strategies for energy efficiency and service provision that consider renewable energy sources, storage and flexible loads will be investigated. It will also explore novel sensor types, inexpensive high-bandwidth communication technologies and security measures based on hardware security modules and blockchain technology to protect communication and services. The project's solution will promote a more environmentally friendly and efficient next-generation energy supply infrastructure.

PROGRESSUS plans to develop a software-defined network enabled, secure communication and metrology platform.

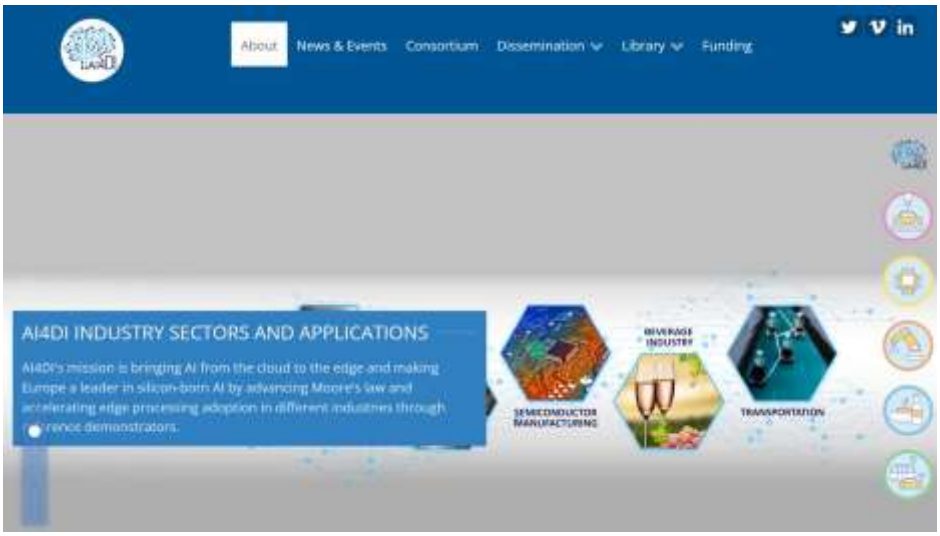
BEYOND5

... and will deeply investigate the inline metrology influences as well as ...

VIZTA

Specific metrology techniques will be further developed within VIZTA in cooperation with ... to insure wafer to wafer bonding quality.

AI4DI



In **AI4DI**, we will deploy AI-based virtual metrology schemes for assessing the quality of products (semiconductor, food, wood) without manual intervention or destructive processes, achieving reduced cost / higher productivity.

A NEW DEVELOPMENT: EUROPEAN CHIPS ACT

https://ec.europa.eu/commission/presscorner/detail/en/ip_22_729

THE EUROPEAN CHIPS ACT

3 Pillars

Chips for Europe Initiative: pool resources from EU, MS and other, as well as the private sector, through: the "**Chips Joint Undertaking**"	**New framework to ensure security of supply** by: A. Attracting **investments** and enhanced **production capacities**. B. **Chips Fund to facilitate access to finance** for start-ups to help them mature their innovations and attract investors. C. D**edicated semiconductor equity investment facility** under InvestEU to support scale-ups and SMEs to ease their market expansion.	**Coordination mechanism between the Member States and the Commission** for monitoring the supply of semiconductors, estimating demand and anticipating the shortages. • **monitor** the semiconductor value chain • **common crisis assessment** • coordinate **actions to be taken** from a new emergency toolbox • **react swiftly and decisively together**

CHIPS FOR EUROPE INITIATIVE

Bridge the gap ***from lab to fab***

Create ***large innovation capacity*** and ***a resilient and dynamic*** semiconductor ***ecosystem***

- Build up **large-scale design innovative capacities** for integrated semiconductor technologies
- Enhance existing and developing new **pilot lines** such as lower nodes sub 2nm, SOI, advanced packaging
- Build advanced technology and engineering capacities for accelerating the development of **quantum chips**
- Create a network of **competence centres** across Europe
- Establish a **Chips Fund** to facilitate access to loans and equity by start-ups, scale-ups and SMEs and other companies in the semiconductor value chains

TAKE AWAY POINTS

KDT is the largest European programme in electronic components and systems.

Metrology is an inherent part of the projects funded by KDT.

Thank you!