

"Europe will not be made all at once, or according to a single plan. It will be built through concrete achievements which first create a de facto solidarity."
Robert Schuman

THE KDT JOINT UNDERTAKING. THE EUROPEAN PROGRAMME FOR RD&I IN ELECTRONIC COMPONENTS AND SYSTEMS.

OPEN CONSULTATION ON METROLOGY FOR SEMICONDUCTOR TECHNOLOGIES



Yves GIGASE
Head of Programmes
08 July 2022

EUROPEAN
PARTNERSHIP

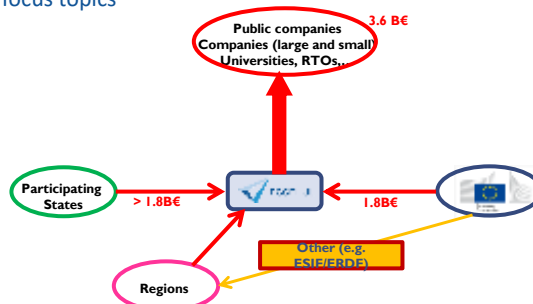


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KDT JU 2021-2027

- Third generation JU (start 30/11/2021), predecessor was ECSEL JU
- KDT JU = Key Digital Technology Joint Undertaking
- Tripartite: Commission - Participating states – Industry associations
- Associations: AENEAS, INSIDE, EPoS
- Budget ambition : 7.2B€ funded by 1,8 B€ (EU)+1,8 B€ (national)
- Based on Horizon Europe
- **Bottom-up** programme with **top-down** focus topics
- “Value chain” approach
- **Pilot lines** (higher TRLs)
- **critical mass** approach
- focussed on **industrial leadership**
- **common agenda of Europe’s ECS**



<https://www.kdt-ju.europa.eu/>



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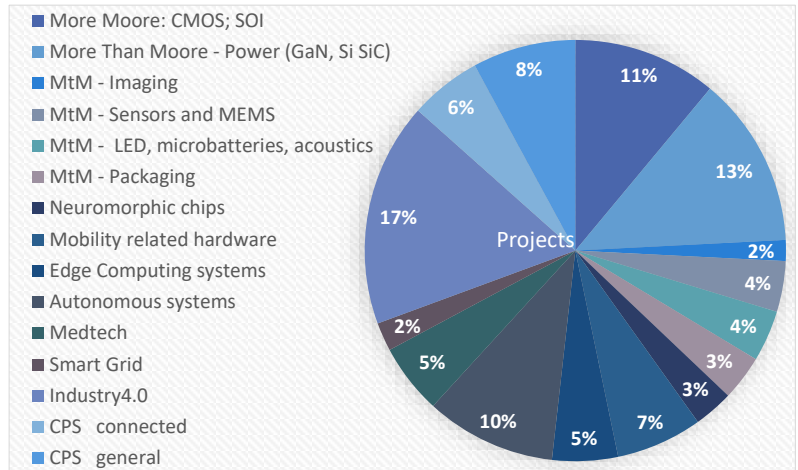
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PARTNERSHIP



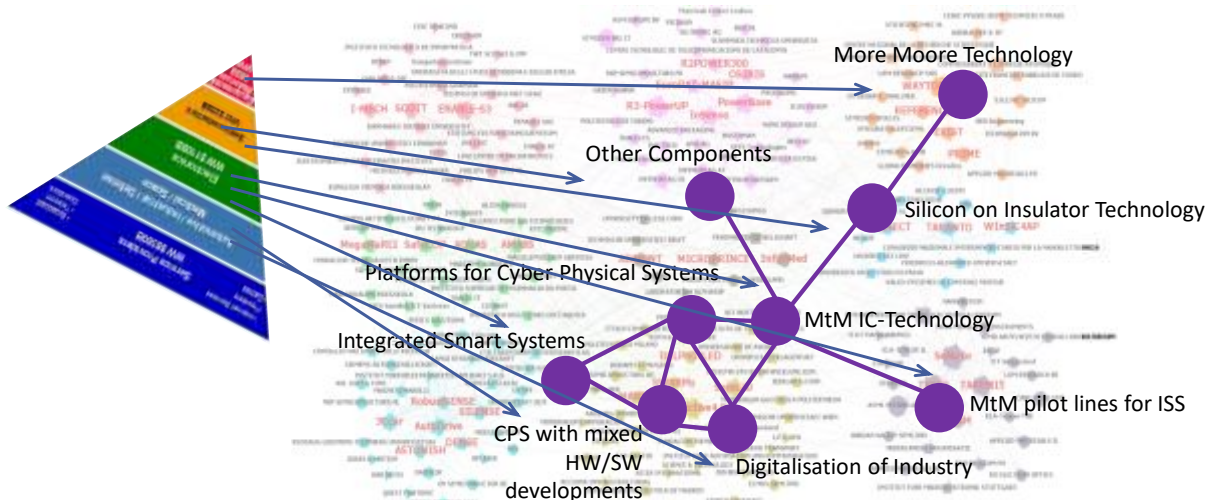
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ECSEL JU 2014-2021

- 92 projects
- 3 220 beneficiaries
- 4 690 million Eur in total cost
- 2 280 million Eur in funding (EU+national)
- 408 500 persons-months
- 29 participating states



NETWORKS OF PARTNERS AND PROJECTS



MORE MOORE PROJECTS

[illegible]

All with participation of PTB




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3DAM



3DAM
Advanced Metrology & Characterisation for 3D CMOS

← PREVIOUS

NEXT →

WORKING GROUP

As nano-electronics technology is moving beyond the boundaries of [strained] silicon in planar or FinFETs, new 3D device architectures and new materials bring major metrology and characterisation challenges which cannot be met by putting the present techniques to their limits.


3DAM will be a path-finding project which suggests and implements several existing and future 3DAM pilot-line projects. It is linked to the IMAP area 71 (Initiative "More Moore"), innovative demonstrators and metrologies will be built and evaluated within the themes of metrology and characterisation of 3D device architectures and new materials, across the full IT manufacturing cycle from front to back End-Of-Line. 3D structural metrology and defect analysis techniques will be developed and combined to address challenges around 3D critical Dimension (CD), strain and crystal defects at the on-scale. 3D compositional analysis and electrical properties will be investigated with special attention to interfaces, alloys and 2D materials.

The project will develop new workflows combining different technologies for more reliable and faster results to be used in future semiconductor processes.

The consortium includes major European semiconductor equipment companies at the state of metrology and characterisation. The link to future needs of the industry, as well as critical evaluation of concepts and demonstrators, is ensured by the participation of IMAP and LETI.

The project will directly increase the competitiveness of the strong Europe-based semiconductor equipment industry. Closely connected European IC manufacturers will benefit by estimated R&D and process cost-ups. The project will generate technologies essential for future semiconductor processes and for the applications enabled by the new technology nodes.

Categories: Smart systems, Integrated, Smart production



Project coordinator:
IMEP-LEDA

Lead:
Dr. Jean-Pierre LÉON

Website:
3DAM.EUROPEAN-PROJECTS.EU

Start date: 01/2016

Duration: 36 months

Total investment: 1M €

Participating organisations:
IMEP-LEDA, IMAP, LETI, STMicroelectronics, ASML, Applied Materials, KLA, Nanoscope, etc.

Number of countries:
10

Advanced Metrology & Characterisation for 3D CMOS

3DAM logo, ECSEL JU logo, Leti logo

Workshop in the frame of the 3DAM European ECSEL Project

March, 15th 2019 - Titane 1 room, Maison MINATEC, Grenoble

As nano-electronics, technology is moving beyond the boundaries of [strained] silicon in planar or FinFETs, new 3D device architectures and new materials bring major metrology and characterisation challenges which cannot be met by putting the present techniques to their limits. 3DAM "3D Advanced Metrology and materials for advanced devices" is an EU-funded pathfinding and assessment project focusing on innovations and progress in metrology and characterisation related to the latest generation of 3D front-end of line (FEOL) and back-end of line (BEOL) structures (3D, nanowires, TSVs) as well as 2D materials.

- Dimensional metrology:** 3D-SPM, CD-SEM, OCD
- Structural analysis:** Electron Tomography, PL & CL, SHG, D3D-SAM, X-ray NanoCT
- Compositional/dopant analysis:** EDS, APT, STEM-EDS and EELS, WDS, AES, HRXED
- Carrier distribution and mobility:** 3D SIMS, micro-matrix probe, TDS, spectroscopy
- Strain and stress:** HRD, Raman, Precision Electron Diffraction in a TEM

The goal of this workshop is to disseminate the results of the projects to the public. The combination with the insights and findings from experts will make this one-day workshop an up-to-date overview of the most recent advances in the analytical techniques and diagnostic capabilities essential for technology development.

Keynote speakers:



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MADEin4

MADEin4

Metrology Advances for Digitized Electronic Components and Systems (ECS) Industry 4.0



THE MADEin4 PROJECT IMPROVES INDUSTRY 4.0 MANUFACTURING PRODUCTIVITY BY DEVELOPING



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EUROPEAN PARTNERSHIP



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PILOT LINE PROJECTS AND PROJECT SUITES

More Moore

The projects contribute directly to the European Strategic Roadmap for Micro- and Nano-Electronics Systems.



SOI



Power components

Description of projects on KDT website
<https://www.kdt-ju.europa.eu/>



Power Semiconductor and Electronics Manufacturing 4.0 smart, security, variation, simulation
excellence in speed and reliability for More than Moore technologies - High volume production and quick introduction

"Enhanced Power Pilot Line": 2nd generation power semiconductor devices on 300mm wafer

"Enabling Power technologies on 300mm Wafers" project was based on the concept of a 1.1 transfer approach from 200 mm to 300 mm diameter silicon wafers.

from ASML



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MATQu

Q-COMPUTING



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POWER2POWER



Providing next-generation silicon-based power solutions in transport and machinery for significant decarbonisation in the next decade

Press release: - European research project Power2Power for more efficient power semiconductors launches in Dordrecht

Example
Development and
implementation of an ultra-
precise wafer thinning process.
Set up an appropriate
metrology and data processing
in this area.



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YESvGaN



YESvGaN will establish a new class of vertical GaN power transistors which combines the performance benefits of vertical Wide Band Gap (WBG) transistors with the cost advantages of established silicon technology. These transistors can replace IGBTs and thus reduce power conversion losses in many price-sensitive applications ranging from power supplies in data centers to traction inverters for electric vehicles. YESvGaN covers the development of the required new technology all the way from wafer to application.

Possible electricity savings in the EU in 2030 by consequent implementation of YESvGaN vertical membrane GaN transistors in the target applications

PROGRESSUS



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Highly Efficient and Trustworthy Electronics, Components and Systems for the Next Generation Energy Supply Infrastructure



Next Generation Smart Grid to reduce Greenhouse Gas Emissions and Grid Peak Power

The high-power requirements of ultra-fast charging stations give rise to special challenges when designing smart charging infrastructure. In support of Europe's 2030 climate targets, the EU-funded PROGRESSUS project aims to introduce a next-generation smart grid demonstrated by the application example of a smart charging infrastructure integrating seamlessly into current smart grid architecture concepts. To do so, it will research new efficient high-power converters that

support bidirectional power flow. New DC microgrid management strategies for energy efficiency and service provision that consider renewable energy sources, storage and flexible loads will be investigated. It will also explore novel sensor types, inexpensive high-bandwidth communication technologies and security measures based on hardware security modules and blockchain technology to protect communication and services. The project's solution will promote a more environmentally friendly and efficient next-generation energy supply infrastructure.

PROGRESSUS plans to develop a software-defined network enabled, secure communication and metrology platform.

BEYOND5



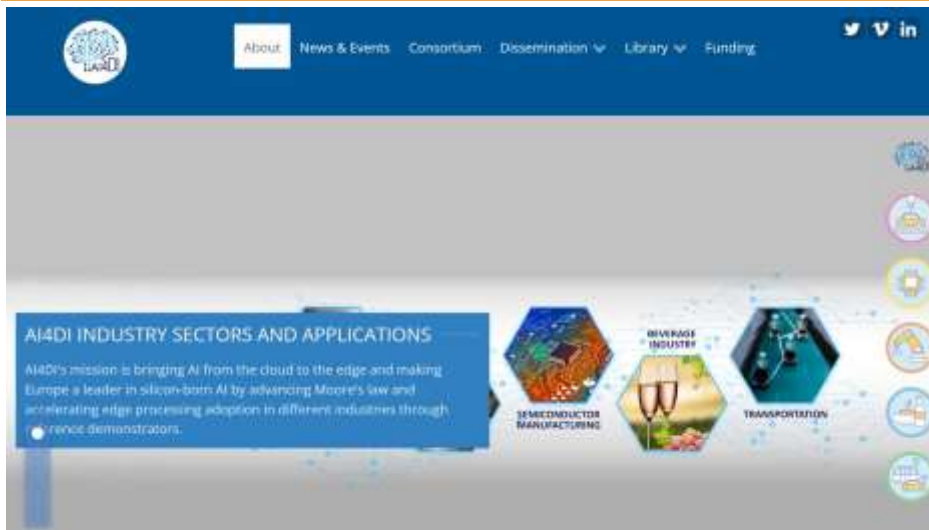
... and will deeply investigate the inline metrology influences as well as ...

VIZTA



Specific metrology techniques will be further developed within VIZTA in cooperation with ... to insure wafer to wafer bonding quality.

AI4DI



In **AI4DI**, we will deploy AI-based virtual metrology schemes for assessing the quality of products (semiconductor, food, wood) without manual intervention or destructive processes, achieving reduced cost / higher productivity.

A NEW DEVELOPMENT: EUROPEAN CHIPS ACT



https://ec.europa.eu/commission/presscorner/detail/en/ip_22_729

THE EUROPEAN CHIPS ACT

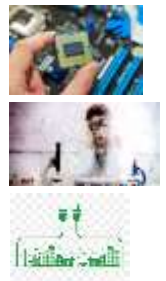
3 Pillars

Chips for Europe Initiative: pool resources from EU, MS and other, as well as the private sector, through: the "Chips Joint Undertaking"	New framework to ensure security of supply by: A. Attracting investments and enhanced production capacities . B. Chips Fund to facilitate access to finance for start-ups to help them mature their innovations and attract investors. C. Dedicated semiconductor equity investment facility under InvestEU to support scale-ups and SMEs to ease their market expansion.	Coordination mechanism between the Member States and the Commission for monitoring the supply of semiconductors, estimating demand and anticipating the shortages. <ul style="list-style-type: none"> • monitor the semiconductor value chain • common crisis assessment • coordinate actions to be taken from a new emergency toolbox • react swiftly and decisively together
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CHIPS FOR EUROPE INITIATIVE

Bridge the gap *from lab to fab*
 Create **large innovation capacity** and **a resilient and dynamic** semiconductor ecosystem

- Build up **large-scale design innovative capacities** for integrated semiconductor technologies
- Enhance existing and developing new **pilot lines** such as lower nodes sub 2nm, SOI, advanced packaging
- Build advanced technology and engineering capacities for accelerating the development of **quantum chips**
- Create a network of **competence centres** across Europe
- Establish a **Chips Fund** to facilitate access to loans and equity by start-ups, scale-ups and SMEs and other companies in the semiconductor value chains



TAKE AWAY POINTS

KDT is the largest European programme in electronic components and systems.

Metrology is an inherent part of the projects funded by KDT.

Thank you!