FINAL PUBLISHABLE REPORT

Grant Agreement number	17IND06
Project short name	FutureGrid II
Project full title	Metrology for the next-generation digital substation instrumentation

Project start date and duration:		01 June 2018 (36 + 4 months = 40 months)
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Internal Funded Partners: 1. PTB, Germany 2. INRIM, Italy 3. TUBITAK, Turkey 4. VSL, Netherlands 5. VTT, Finland	External Funded Partners: 6. CIRCE, Spain 7. COMSENSUS, Slovenia 8. RSE, Italy 9. STRATH, United Kingdom 10. SUN, Italy 11. Synaptec, United Kingdom 12. UNIBO, Italy	Unfunded Partners: 13. METAS, Switzerland
RMG: -		

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1 Overview

To support the European electrical power industry, this project provided missing solutions for the calibration and the timing of the new type of substation instrumentation according to IEC 61850 to accomplish the objectives for “establishing calibration methods to support testing of digital instrument transformers”, “providing references for instruments with digital input or output”, “developing tools for devices that exploit sampled values in digital substations” and for “developing traceable references for the verification of time and synchronisation methods”. The project also supported standardisation organisations in their work on new or revised standards that will enable more precise measurements in the future.

2 Need

The decarbonisation of energy systems has been causing significant and unprecedented changes in electrical power grids, due to the wide-scale introduction of decentralised renewable energy resources. Consequently, future electrical power grids have required real-time capable control and monitoring systems to ensure stability under increasingly complex and challenging conditions. The associated digital high voltage sensors and digital metering systems had to be managed through accurate and reliable time synchronisation in a wide area. This was reflected in project Objective 4.

New standards in the IEC 61869 had previously been published for low power instrument transformers (LPIT) or were expected to be released for the electronic current and voltage transformers in the future, as well as for stand-alone merging units (SAMU) in 2018. Due to the introduction of these new standards, the movement from traditional analogue instrument transformer (IT) technology towards the new digital instrumentation technology was expected to gain speed, both on transmission (>100 kV) and on distribution (<100 kV) level. To support this change, new metrological tools and methodologies were needed. The need to provide test systems for new LPIT and SAMU technology was addressed in this project in Objectives 1 and 2. Also, test systems were needed to prove performance of intelligent electronic devices, like digital energy meters or real-time critical all-digital PMU’s. This was addressed in this project in Objective 3. Lastly, to enable industrial uptake and uniformity, active support of standardisation organisations was required, which was addressed in Objective 5.

3 Objectives

The overall objective of this project is to develop the necessary metrological infrastructure for closing the gap in the traceability chain between measurements made in fully digitally operated substations and the realisation of the relevant units in National Metrology Institutes. This includes characterisation of required industrial products, e.g. digital phasor measurement units, digital instrument transformers and sensors and to provide proposals for implementing time stamping of sampled values according to IEC 61850-9-2 using alternate time dissemination protocols in substation. This is required for the successful transition of the present electricity grid towards a modern future power grid.

The specific objectives of the research were:

1. To establish **calibration methods to support dynamic testing of digital instrument transformers** (IT) for rated voltages up to 400/√3 kV and at least 2 kA. In addition, to support technology integration into digital substations, including real-time monitoring systems associated with power quality (PQ) and synchrophasor measurements with uncertainties from 30 ppm under laboratory conditions and up to 0.1 % under on-site conditions.
2. To develop **reference standards for the calibration of instruments with digital input or output to support the transition to digital substations**. Such devices to be tested are stand-alone merging units, which are disciplined by either GPS or PTP or digital measuring instruments (e.g. energy meters). This includes studies on synchronisation of sampling processes, on increasing sampling rates beyond those specified in IEC standards, and on the accuracy of distributed digital power measurements.
3. To develop metrological **tools for the characterisation of devices that exploit sampled values in digital substations**, for the verification of all-digital power and power quality meters and phasor measurement units (PMUs). This includes e.g. studies on limitations due to latency and computation time, and characterisation of error sources in order to provide proposals for an enhanced protocol for sampled values.

4. To develop **traceable reference standards for the verification of UTC time dissemination and synchronisation methods**. This includes study on techniques and algorithms such as PTP and White Rabbit for the synchronisation to a common time reference, both within and between digital substations. In addition, to carry out studies on secure protocols for time dissemination. To develop and validate satellite-independent PMU utilising distributed sensors.
5. To **facilitate the take up of the technology and measurement infrastructure developed in the project.** Target stakeholders included the measurement supply chain (instrument manufacturers), standards developing organisations (IEC TC38 WG 55, IEC TC57 WG 10, IEEE TC39, IEEE P1588) and end users (energy distribution companies).

4 Results

4.1 Objective 1

Objective 1 is to **create** and **establish calibration methods** to support dynamic **testing of digital instrument transformers (IT)** for rated voltages up to 400/√3 kV and at least 2 kA. In addition, to **support technology integration** into digital substations, including **real-time monitoring systems** associated with power quality (PQ) and synchrophasor measurements with uncertainties from 30 ppm under laboratory conditions and up to 0.1 % under on-site conditions.

Overview of the most remarkable results for this objective

First, a novel database of relevant high voltage waveforms associated with power quality measurements, based on real phenomena, was set up. The programmable and time-synchronised high voltage and high-current generation up to 100 kV and 2 kA, capable of producing these PQ relevant waveforms has been integrated in partners measuring systems. Whereas waveform generation of complex low-level signals is not a new field, but the application to, and implementation with the high voltage and high current testing for instrument transformers and sensor can be considered new in Europe.

Second, measuring systems for current- and voltage sensors were set up at different partners. The measurement-related functions for calibrating digital voltage or current transformers and the associated time synchronisation to PPS via either PTP (IEEE 1588), IRIG-B or GPS based time receivers were made ready. In summary, the current sensor calibration system can measure with basic uncertainties of 30 ppm and 60 µrad. The voltage sensor calibration system can handle voltages up to 100 kV with basic uncertainties of 50 ppm and 50 µrad. One existing high voltage facility can handle the extend range 400/√3 kV with the developed measuring systems. Before the *FutureGrid II* project, only some institutes in Europe or even worldwide had been able to offer calibration services in this field at all, and the uncertainties in this field had been higher than 100 ppm (or µrad).

Further, a new (first-in-the-world) universal comparator was finalized, able to compare any type of voltage or current sensor even in the presence of PQ / PMU events within a frequency spectrum up to 9 kHz. Further developments have yielded another device, capable of carrying out a real-time calibration of large digital instrument transformers installed at the substation busbars by comparison to a traceable voltage transformer, and also with the completely new capability of simultaneously analysing tens of different sampled value data streams to obtain a distributed PQ measurement functionality within a smart substation.

Additionally, a multi-purpose calibration system for on-site measurements was built. Each part of the system can be used individually for current or voltage transformer calibrations, including those with digital outputs. The setup including the comparator used for the calibration under current harmonics up to 50th order was characterized with the uncertainty of well below 200 ppm which is far better than the targeted uncertainty of 0.1%. This substantially improves previous state of the art capabilities in Europe.

Furthermore, several recommendations have been contributed to the new standard developed in IEC TC38 / IEEE TC39 WG55 “IEC/IEEE TS 61869-105 ED1 - Instrument transformers - Part 105: Uncertainty evaluation in the calibration of Instrument Transformers” and to IEC TC38 WG 47 on evolution of instrument transformer requirements”. The standard IEC/IEEE TS 61869-105 ED1 is in the moment in the status of a committee draft (CD). Three partners have planned to submit new or enhanced CMCs on calibration services for non-conventional (i.e., even digital) instrument transformers.

Several paper on the findings of the objective-related work have been published – see reference section.

Creation of **calibration systems** for **testing of digital instrument transformers**

The setup of the PTB system, shown in the figure below, for current transformer (CT) calibrations can handle currents up to 2 kA. The setup is mainly made up of a high current generation system, a set of 4 analogue reference current transformers with rated currents of 50 A (CT50), 200 A (CT200), 600 A (CT600) and 2 kA (CT1500) and with associated precision resistors from 1 Ω to 20 Ω and a precision two-channel measuring system. The synchronization signals are necessary when the output of the device under test (DUT) is a sampled value data stream (SVs). The synchronization signals can be obtained by GPS receivers and be transmitted as 10 MHz, pulse per second (PPS) and IEEE 1588-2008 (PTPv2). The system offers a basic uncertainty of 20 ppm for the ratio error and 30 µrad for the phase error under laboratory conditions.

This PTB system is a traceable calibration system for conventional or non-conventional current sensors even with digital output. Details of the system components are presented in the following. The absolute phase errors of the two-channel generator related to the pulse per second time reference of the global positioning system can be configured to almost zero. The accuracies of the reference current transformers are within ±10 µA/A and µrad at power frequency. The sampled value receiver box is validated for the sample rate of 4 kHz according to the IEC standard 61869-9.

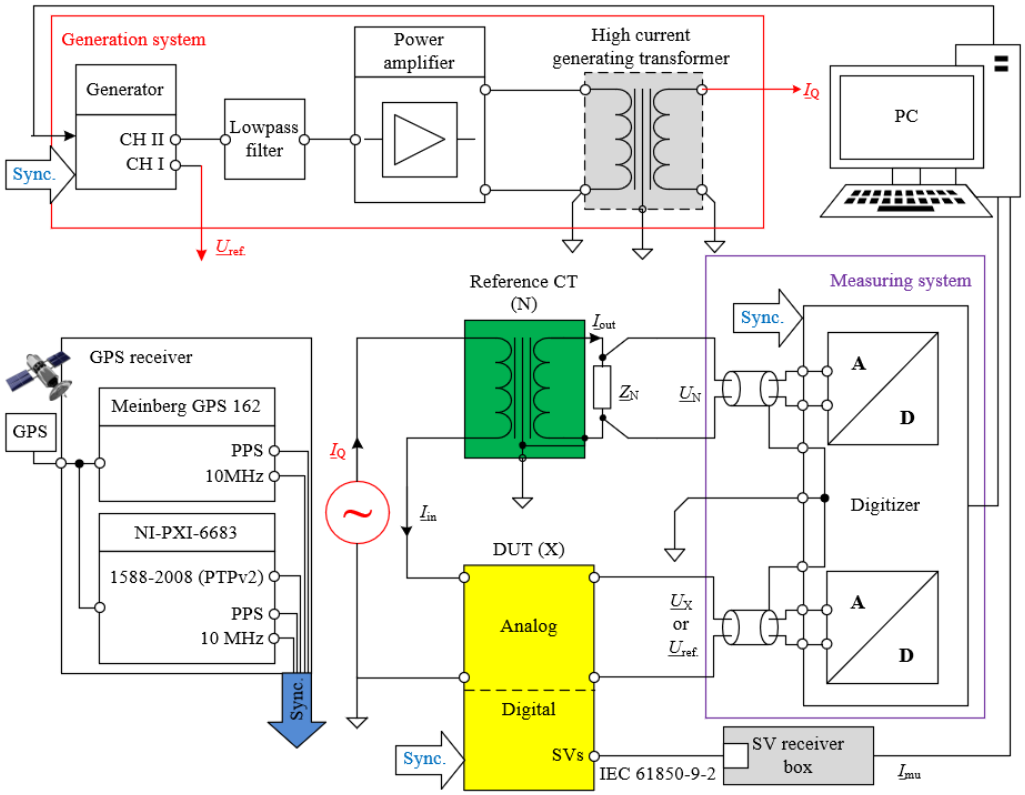

Figure: The setup of the PTB calibration system for current transformer

At INRIM, starting from the hardware used for the medium voltage, voltage transformer frequency response characterization, a suitable measurement setup was developed. The block diagram and the setup used at INRIM for voltage transformer (VT) characterization are shown at the left and right, respectively of the Figure below. The test waveform is generated by an Arbitrary Waveform Generator (the NI PXI 5422, 16-bit, variable output gain ± 12 V, 200 MHz maximum sampling rate, 256 MB onboard memory). The chassis 10 MHz PXI clock is used as reference clock for its high-resolution phase locked loop circuitry. The generation frequency of the AWG is therefore chosen to be an integer multiple of the generated fundamental frequency. A second AWG is used to generate a 12.8 MHz clock, which is used as a time base clock for the signal comparator. As described in [12], The low voltage waveform from the AWG is amplified by a Trek high-voltage power amplifier (30 kV_{peak}, 20 mA_{peak}) with wide bandwidth (from DC to 2.5 kHz at full voltage and 30 kHz at reduced voltages), high slew rate (<550 V/µs) and low noise. Applied voltage reference values are obtained by means of a 30 kV wideband reference divider (VT_{REF} in Fig. 3) designed, built, and characterized at INRIM.

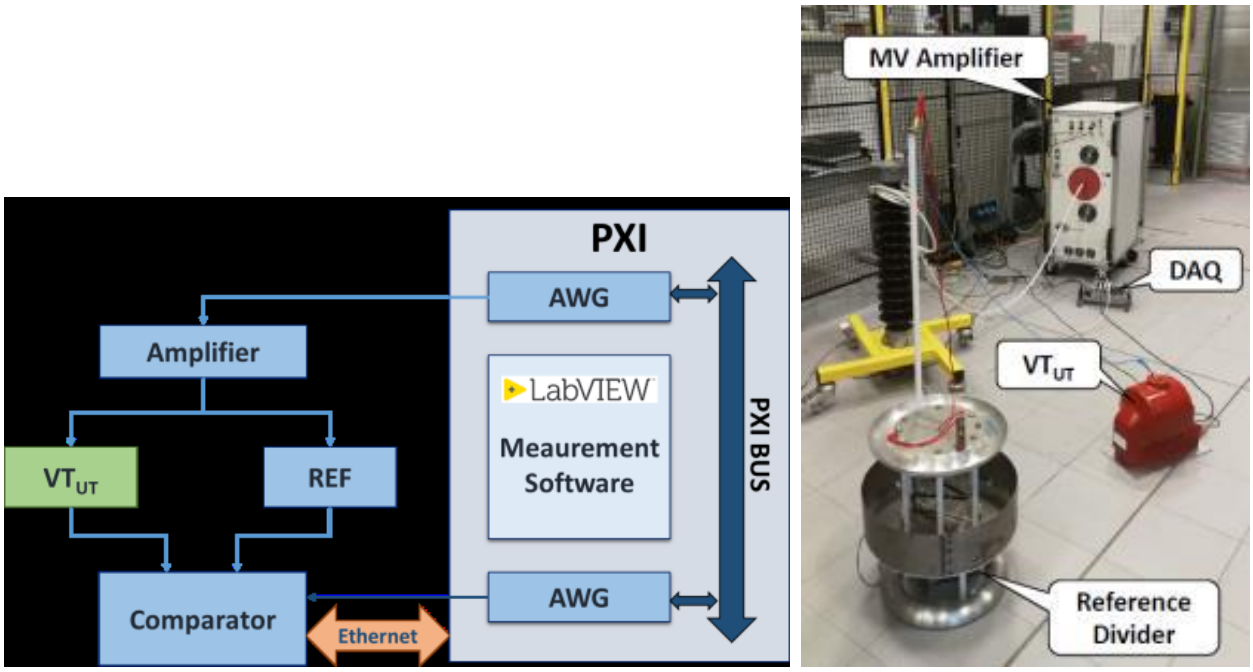

Figure: Setup for the VT characterization: left) block diagram, right) experimental test bench at INRIM.

The acquisition system is a NI cDAQ chassis with four acquisition modules: NI 9225 (± 425 V, 24 bit, 50 kHz), NI 9227 (± 14 A, 24 bit, 50 kHz), NI 9239 (± 10 V, 24 bit, 50 kHz), NI 9238 (± 500 mV, 24 bit, 50 kHz). Expanded uncertainty (confidence level 95%) is 0.007% for the ratio error and 0.07 mrad for the phase up to 1 kHz 0. The sampling clock of the digital comparator is derived from the 12.8 MHz time base clock so that generation and acquisition are synchronized. The software for data processing and instrument control is developed in LabVIEW. A large variety of signals can be generated, such as sinusoidal, fundamental plus a harmonic tone, fundamental with *N* harmonics, fundamental with an inter-harmonic, modulated signal, frequency ramp, transient, typical PQ events etc. The VT primary and secondary voltage are acquired with f_s=50 kHz sampling frequency and 20 s acquisition time.

Finally, at INRIM, two different voltage generation and measurement setups for different voltage levels are used for the calibration of Low Power Voltage Transformers (LPVTs). The first is for voltages up to 20kV (rms), while the other is for 20kV to 100 kV. Both these systems include generation and measurement sections based on a National Instruments (NI) PCI eXtension for Instrumentation (PXI) platform. The two systems differ in the generation and reference systems whereas the same acquisition systems and synchronization set-ups are used. The attained best possible uncertainties for voltage transformer calibration are 50 ppm and 50 µrad.

TUBITAK UME designed a multi-purpose calibration system for power frequencies. On the one hand, it can be configured for high power measurements and transformer loss measurements (see the following block diagram figure) by operating the voltage and current parts of the system synchronously, on the other hand each part of the system can be used individually for current or voltage transformer calibrations, including current and voltage transformers with digital outputs. The on-site current transformer calibration setup consists of a signal generation unit (sinusoidal waveform and harmonics), power amplification with linear amplifier(s), transconductance power amplification (converting voltage power to high current) and measurement part with reference transformer(s) and bridge(s). For sinusoidal waveforms the bridge is a commercial one (ZERA WM3000I) while a PXI chassis with NI4461 ADC and reference shunt are used for non-sinusoidal waveforms (for current harmonics here).

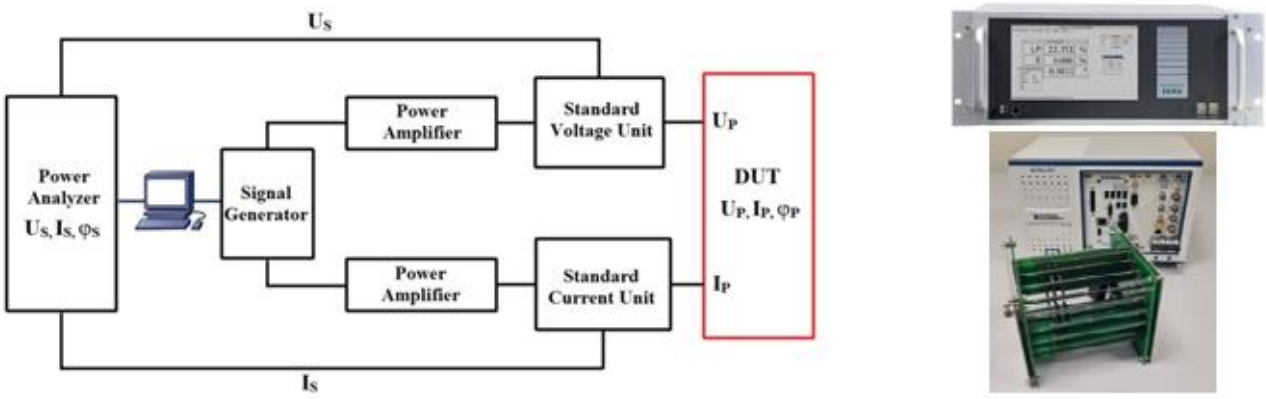

Figure: Block diagram of calibration system for high power. ZERA WM300I Bridge for current transformers with digital output for sinusoidal waveform and PXI-chases with NI4461 unit for harmonics (on the right).

The bridge (ZERA WM3000I) used for sinusoidal waveforms could be calibrated of its full input range with the best uncertainties of;

- 5 ppm (and 5 µrad) for unity ratio from 5% up to 200% of nominal currents (for current-to-current comparison - ICTs)

- 20 ppm (and 20 µrad) for unity ratio from 5% up to 200% of nominal currents and nominal voltages (for current-to-voltage comparison – LPCTs with analogue output)

- 100 ppm (and 100 µrad) for unity ratio from 5% up to 200% of nominal currents and SV data (for current-to-SV data comparison – LPCTs with digital output)

On the other hand, the bridge (digitizer 4461 with shunt) used for transformer calibration under current harmonics up to 50th was characterized with the uncertainty of well below 200 ppm which is quite better than the targeted uncertainty of 0.1%. The uncertainties in the characterization and verification of reference transformers were not above few ppms. This substantially improves previous state of the art on-site capabilities in Europe.

Support of real-time monitoring systems in digital substations

CIRCE designed and constructed a system capable of characterizing on-site digital instrument transformers from the analysis of the IEC 61850/IEC 61869-9 frames injected by the Stand Alone Merging Units (SAMU) located in digital substations. Besides, exploiting the interesting feature of being able to calculate the Power Quality (PQ) from the information sent by the SAMU, the second objective of this work was to implement a suitable computation architecture to monitor distributed PQ nodes. In a first step, this approach relies on the implementation of a IEC 61000-4-30 class-A PQ library on an industrial-based computer. Later, the library is migrated to a more limited platform to identify the maximum number of parallel nodes that the analyser can process. Several experimental tests were carried out to verify the suitability of the proposed solution. The excellent results of the calibration by comparison between the digital instrument transformer and the analogue reference transformer and the number of parallel nodes that the system can analyse indicate that the proposed low-cost analyser meets the stringent class-A requirements of the IEC 61000-4-30 for real-time evaluations.

As indicated, this work includes two main aspects: the first comprises the development of a device capable of making a real-time calibration of large digital instrument transformers installed at the substation busbars by comparison to a traceable voltage transformer (VT). This process is illustrated in the Figure below where one analogue VT, connected to one SAMU, sends digital information through SV to the proposed system. Moreover, the traceable VT is placed near the equipment to be calibrated (typically measuring the same line and close to the EUT to avoid effect line distortions).

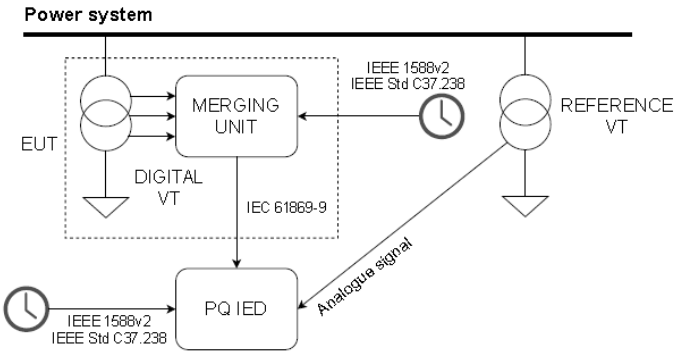

Figure: Calibration of digital instrument transformers by comparison.

This traceable voltage transformer standard is connected to the PQ IED, concretely to a 24-bit high-resolution input with a sampling rate of 50 kSPS. Both systems (the EUT and the reference VT) are synchronized by the same IEEE 1588v2 time source to guarantee that the timestamps of both digital and analogue data are comparable and so the derived PQ results. The second objective is devoted to develop and test a system capable of analysing tens of different SV streams to obtain the distributed PQ within the smart substation. The core of this analysis relies on the design of different IEC 61000-4-30 class-A libraries to be implemented in the IED. Concretely, the algorithms implemented followed the rules included in, including the following: power frequency, magnitude of the supply voltage, flicker, voltage dips, swells and interruptions, voltage harmonics/interharmonics, RVCs and voltage unbalance. Special attention was paid to the aggregation process as each SV stream must be analysed individually as an isolated three-phase system to ensure a proper comparison between SAMUs. In this regard, every SAMU must be synchronized by a common time source. An illustrative general block diagram of an installation with distributed SAMU and their connection to the proposed system is shown in the Figure below.

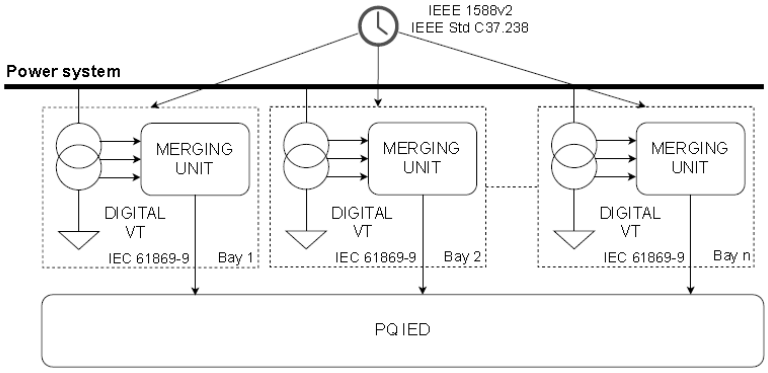

Figure: Multi-point real-time monitoring systems with IEC 61850 Power Quality assessment in digital substations.

SUN developed and characterized a "universal" comparator able to compare any type of transducer, voltage or current output, conventional / unconventional, analogue / digital, in the presence of PQ / PMU events with frequency spectrum up to 9 kHz. Analogue inputs from ± 500mV to ± 450V for voltage and ± 20 mA to ± 50 A for currents are considered, as well as digital input for both voltage and optic. It works with GPS or a different sync pulse. Regarding the uncertainties, 100 ppm for magnitude and 150 µrad for phase are the target uncertainties up to 9 kHz.

All clock and synchronization signals are generated by the NI PXI-6683H timing and synchronization module, see Figure below. In particular, the oversampling clock of the voltage and current modules, generated by NI PXI-6683H, is supplied externally to NI cDAQ, through the PFI0 terminal (Programmable Function Input 0). It should be also noted that the voltage and current modules start sampling when they recognize the first rising edge of the oversampling clock, after initialization and start-up. This allows AD converter synchronisation based on delta-sigma architecture.

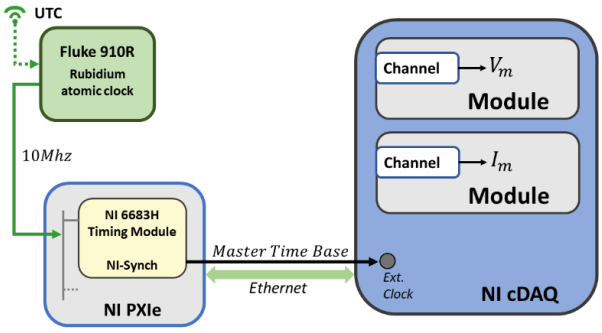

Figure: shows the universal comparator scheme.

The NI6683H is also able to implement PTP protocol in order to provide absolute time reference to the devices under test which are digital low power instrument transformers (DLPIT) or SAMU coupled with inductive transformers.

The universal comparator was developed in a modular way. In order to compare transducers with analogue voltage/current output, analogue modules shown in Table 3.2.1, based on National Instruments CompactDAQ chassis, which is an 8-slot chassis designed for distributed or remote measurements, have been employed.

Table: Universal Comparator Voltage and Current modules

Voltage		Current	
Module	Range	Module	Range
NI 9238	±500mV	NI 9203	±20mA
NI 9239	±10V	NI 9227	±7A
NI 9225	±450V	NI 9247	±70A

All voltage and current modules are based on delta-sigma architecture (24 bits resolution), whose sampling rate (max 50 kHz) depends on the internal/external master time base. In order to increase current and voltage steps, it is possible to use a current or voltage reference transducer. For example, the A40B Series Precision DC and AC Current Shunts and a voltage divider have been used for this aim.

Overall, the conclusion of these activities, represent the finalisation of the technical aspects (calibration methods and -systems for currents up to 2 kA under laboratory and on-site conditions with sufficient uncertainties, albeit for voltages up to 200 kV instead of the targeted 400/√3 kV) of Objective 1.

Support technology integration in digital substations (see also impact section)

UNIBO supported technology integration by highlighting open issues in a publication for scientifically discussing future Standardization of Limits to Offset and Noise in Electronic Instrument Transformers. The scenario of instrument transformers has radically changed from the introduction of the Low-Power version, both passive and active. The latter type, typically referred to as Electronic Instrument Transformers (EITs), has no dedicated standard within the IEC 61869 series yet. To this purpose, UNIBO proposed and discussed the understanding on how the limits of typical disturbances affecting EITs should be standardized. In particular, a mathematical approach has been presented to determine the sources of signal disturbances influence, which affect the rms value and the ratio error. From the results, it has been discussed that the emergence of disturbances generated within the EIT is a critical aspect to be studied with data of typical off-the-shelf devices. Therefore, to guarantee a correct operation of the devices, a proper standardization of the sources of disturbance should be provided. In the following UNIBO has led the involvement in the activity of the IEC TC38 WG37 of the new IEC 61869-7 (Low Power Electronic Voltage Transformer) and IEC 61869-8 (Low Power Electronic Current Transformer). This has led to tangible progression in the development of standards. Both standards include analogue and digital output of Low Power Instrument Transformers. Both are forecasted for publication in December 2022.

Furthermore, several recommendations have been contributed to the new standard developed in IEC TC38 / IEEE TC39 WG55 “IEC/IEEE TS 61869-105 ED1 – Instrument transformers - Part 105: Uncertainty evaluation in the calibration of Instrument Transformers” and to IEC TC38 WG 47 on evolution of instrument transformer

requirements". The standard IEC/IEEE TS 61869-105 ED1 is, as of November 2021, in the status of a committee draft (CD).

Lastly, effort has been made to prepare new CMC entries. Here, INRIM and PTB intend to submit extended or modified CMC on non-conventional sensors at the next CMC run next spring. TUBITAK intends to submit new CMCs in parallel with the submissions to TURKAK Accreditation Agency on non-conventional sensors at the 2023 CMC run.

The conclusion of these standardization and CMC related activities represents the finalisation of the facilitation and distribution part (to establish the calibration methods) of Objective 1.

Conclusion

The combined expertise from several partners (SUN, INRIM, PTB, CIRCE, RSE, UNIBO) allowed to effectively cooperate for many joint papers. Exemplarily, in one published paper, a set of different types of instrument transformers has been measured with the described calibration systems.

Overall, the conclusion of these achievements represents the finalisation of all aspects of Objective 1 by the project consortium.

4.2 Objective 2

To develop reference standards for the **calibration of instruments with digital input or output**, in order to support the transition to digital substations. This included studies on **increasing sampling rates** beyond those specified in IEC standards, and on the **accuracy of distributed digital power measurements**.

Overview of the most remarkable results for this objective

First, a reference SAMU was built on a collaborative design of a self-built digitizer for the reference SAMU as well as for a distributed digitizer. The partners calibrated the reference SAMU, based on a new method developed for calibrating the delay of the analogue front ends of the internal ADC cards. The "*Good Practice Guide on the performance of the reference standard SAMU as a calibration reference for the calibration of instruments with digital input or output*", describes this new method for analogue front-end delay calibration of a reference SAMU from this objective. With this setup, an overall uncertainty of 10 ppm and about 28 ns (around 10 µrad) was achieved. Before the *FutureGrid II* project, no such reference SAMU had existed, and no institute worldwide would have been able to offer calibration service for one. This accuracy fully satisfies requirements as a reference standard with respect to the defined error class of commercial SAMUs down to the class 0,05. The reference SAMU and other project-developed references for SAMUs have already been used as references for multiple customer calibrations.

A three-phase set of active current clamps for conventional CTs with rated secondary currents of 1A or 5A as an option for the reference SAMU were developed. The calibrated results of three active current clamps were below 0.015 % for the ratio errors and below 0.04 crad for the phase error. The uncertainties of the calibration results are 50 ppm and µrad (k = 2). Another self-built current clamp with a splitable magnetic core and a 3D printer was used for the fabrication of the current clamp case, with much better errors of below 30 ppm and µrad and improved uncertainties could be obtained. All of this constituted an improvement over the state-of-the-art before the project.

Furthermore, asynchronous sampling processes of the Sampled Values have been simulated. Several resampling algorithms have been developed and evaluated. One of these algorithms is enhanced with respect to the known published algorithms and is capable to achieve an uncertainty that is negligible (far below 10^{-6}) in context to the other uncertainty contributions of the system.

Several paper on the findings of the objective-related work have been published – see reference section.

Reference SAMU for the calibration of instruments with digital input or output

The VTT setup for calibrating IEC 61850-9-2 compliant devices, which either generate or receive SV streams is based on a reference sampling power standard that has been equipped to produce an SV stream from its ethernet port. Samples in the stream have a calibrated magnitude and signal path delays are compensated by adjusting the sample clock delay with respect to the reference 1PPS input. The Figure below shows the front

panel of the device with important input connectors highlighted. The Table outlines the most important technical specifications of the device.

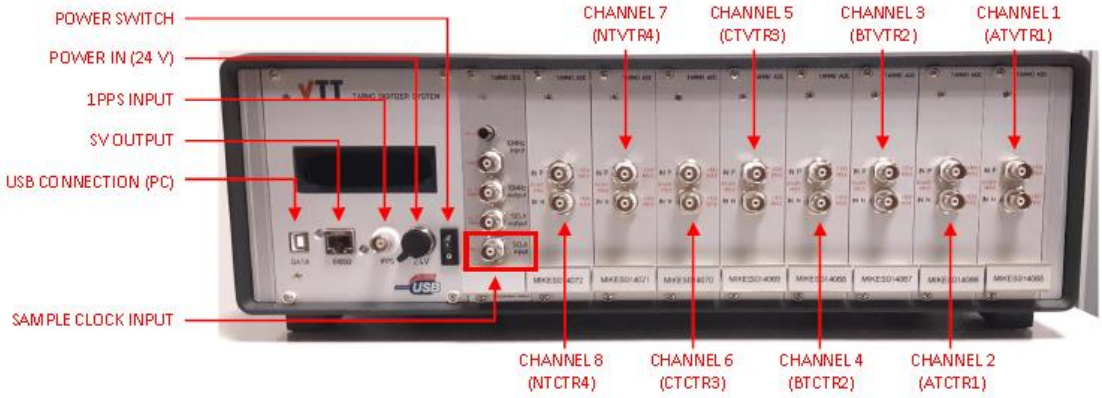

Figure: Front panel and connectors of the reference sampling power standard.

Table: Technical specifications of the reference device.

Property	Value
Input range	± 10 V pos/neg inputs, ± 8 V differential, 2 kV max to GND
SV output streams (from IEC 61869-9)	F4000S1I4U4 (4000 SPS, 1 ASDU, 4x current + 4x voltage) F4800S1I4U4 (4000 SPS, 1 ASDU, 4x current + 4x voltage) F4800S2I4U4 (4000 SPS, 2 ASDUs, 4x current + 4x voltage) F12800S8I4U4 (4000 SPS, 8 ASDUs, 4x current + 4x voltage) F15360S8I4U4 (4000 SPS, 8 ASDUs, 4x current + 4x voltage) F14400S6I4U4 (4000 SPS, 6 ASDUs, 4x current + 4x voltage)
Sample clock input	0 to 5 V rising edge, high impedance
1PPS input	0 to 5 V rising edge, high impedance

For the reference SAMU, a common design and hardware setup of the ADC channels has been worked out between VTT and VSL for the use in the reference SAMU as well as for the distributed digitizer. In the figure below this common design of ADC is shown.

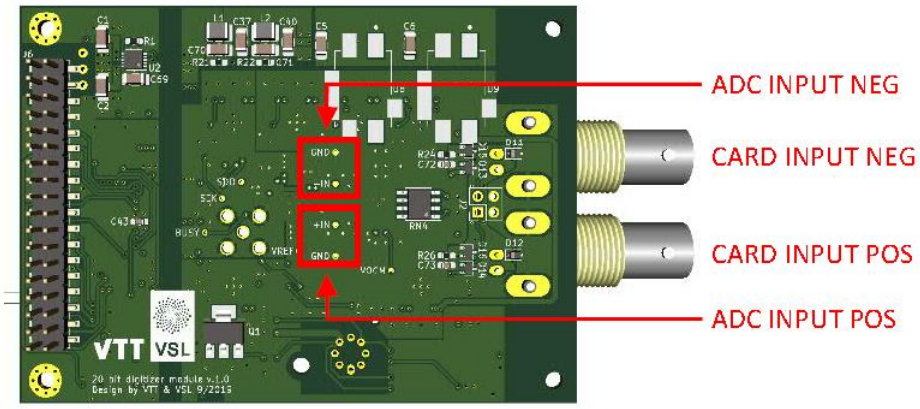

Figure: ADC board bottom view. This represents a common design between VTT and VSL.

The "*Good Practice Guide on the performance of the reference standard SAMU as a calibration reference for the calibration of instruments with digital input or output*", describes this new method for analogue front-end delay calibration of a reference SAMU from this objective. With this setup, an overall uncertainty of 10 ppm and about 28 ns (around 10 µrad) was achieved.

Three active current clamps were designed and developed from PTB for conventional CT's with rated secondary currents of 1A or 5A as an option for the reference stand-alone merging unit (SAMU). The active current clamp was made up of a passive current clamp from Chauvin Arnoux, a self-built electronic error compensation and a precise measuring resistor. Eventually, the electronic error compensation with the precise measuring resistors was built up in a box for three active current clamps. The final accomplished three active current clamps are presented in the figure below (right).

The calibrated results of three active current clamps were below 0.015 % for the ratio errors and below 0.04 crad for the phase error. The uncertainties of the calibration results are 50 ppm and µrad (k = 2). In order to investigate whether a self-built current clamp has the potential to obtain better error characteristic, PTB has constructed a current clamp. For the construction of the self-built current clamp, a splitable magnetic core and a 3D printer was used for the fabrication of the current clamp case. Figure below (middle) shows the accomplished self-built current clamp and Figure below (right) shows a view of the internal construction.

The calibration results of the self-built active current clamp for the 5 A range at power frequency are within 0.0025 % and 0.0022 crad. This proves that the self-built clamp is around 10 times more accurate.

Figure: Left) 3-phase active operated commercial current clamps.
Middle) Self-built current clamp using 3D printer.
Right) Internal core construction of the self-built clamp

Synchronization of sampling processes with various sampling rates

Furthermore, asynchronous sampling processes of the Sampled Values have been developed and simulated by PTB. Several resampling algorithms have been developed and evaluated. One of these algorithms is capable to achieve an uncertainty that is negligible (well below 10^{-6}) in context to the other uncertainty contributions of the system. Sampling-based calibration systems for calibrating "SampledValue" (SV)-based instruments for substation automation require synchronised and time-aligned sampling processes. As the signal frequency of the power grid is always asynchronous to the standardised sampling frequencies according to IEC 61869-9, the sampled waveforms of the calibration system and of the SV-based device under test can be resampled to be synchronised and to allow better accuracy in the following measurements based on the Discrete Fourier Transform (DFT) of the resampled waveforms. The work from PTB presents simulations and results for different resampling algorithms. The scheme of the realised resampling process has been shown in the figure below.

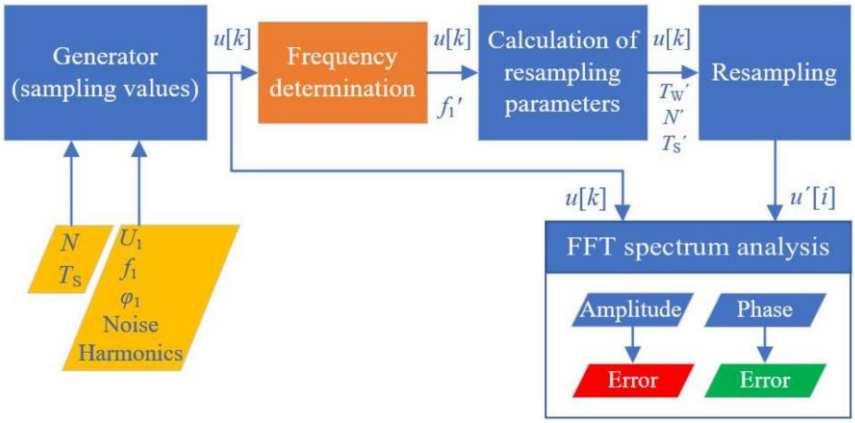

Figure: Schematic of the resampling process.

A modified sinc interpolation method with a finite impulse response (FIR) has been presented – see figure below). The resampling based on the modified sinc algorithm takes the longest computation time, compared to the other two algorithms based on a quadratic and cubic algorithm. The results of the modified sinc resampling algorithm are the most accurate within a normalised bandwidth of up to 40% of f_S.

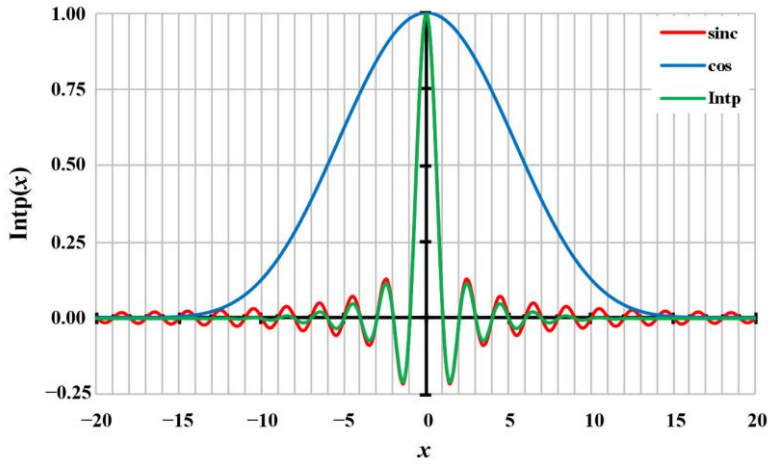

Figure: The composition of the interpolation kernel Intp(x) (green curve) can be seen by the pure sinc function (red) and the modifying $\cos^q$ function (blue curve) for NF = 40 and q = 6.

Even with strongly distorted waveforms, the amplitude and phase errors of the modified sinc algorithm are well below 10 ppm and µrad with signals of up to 40% of f_S. The deviation of the results for the RMS and phase angle is in the order of 10^{-8} V/V (or rad) for normalised frequencies of up to 20% of the sampling frequency. No practical degradation in the presence of noise and harmonics could be observed. To sum up, the results of the modified sinc interpolation method with the phase synchronisation were simulated for typical sampling settings of sampled value-based digital instrumentation in high voltage substations. As the simulation results showed, the proposed resampling process allows the synchronisation of the sampled values to PPS with almost mathematically perfect accuracy. In addition, the experimental results based on the microcontroller-based SV devices confirmed that the proposed modified sinc interpolation method works with SV-based instrumentation as well. The simulations and experimental results allow the highly accurate implementation of the proposed resampling process in the future SV-based calibration systems for SV-based instrumentation, such as digital instrument transformers, SAMUs and digital energy meters. As an example, the highest accuracy class of a SAMU is 0.05. Calibration systems for such a SAMU should be an order of magnitude more accurate. With the modified sinc interpolation method, no practical degradation of the measurement uncertainty through different sampling processes in the device under test (i.e., the SAMU) and the reference (i.e., the calibration system) is to be expected. As a consequence, the modified sinc interpolation method is currently adapted to a calibration platform in the laboratory for the current transformer measuring system. Based on the accurate processing of the digital signal quantities by using the modified sinc resampling algorithm, further power-quality-related calibrations will be accomplished in the future.

Distributed digital power measurements

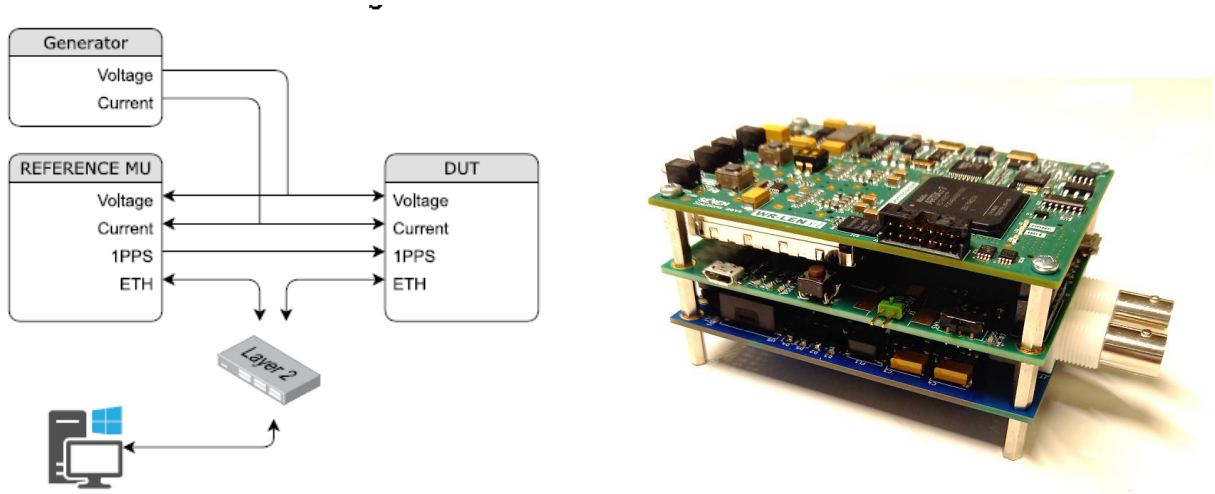

Figure: Left) The VSL concept where the MU is generating the 1 PPS. Right) VSL realisation for the distributed digitizer, to allow distributed power measurements.

The VTT concept of the reference SAMU has been turned around into the VSL concept (see figure above), which is to let the reference merging unit (MU) generate the reference clock (1 PPS). This circumvents that the reference clock needs to be synchronized to the 1 PPS. This synchronization can sometimes be the dominant uncertainty contribution in the phase displacement uncertainty budget. But for the calibration of other merging units (or in this case a distributed digitizer for power measurements) it is not necessary to synchronize to GPS or other time services, if a local 1 PPS is generated.

The reference merging unit used in this manner is built on commercially available hardware and the software. This makes it less dependent on custom build components and makes it available for others to implement as well. The table below shows the components used.

				
Controller	Ni9225 Voltage input 3-Channel, 300 Vrms, 24-Bit Simultaneous, Channel-to-Channel Isolated Analog Input Module	Ni9246 Current input 3-Channel, 20 Arms Continuous, 24-Bit, Analog Input Module	Ni9402 Trigger outputs 4 DIO, LVTTL, Bidirectional, 55 ns	Ni9269 Voltage output 100 kS/s/ch Simultaneous, ±10 V, Isolated, 4-Channel

The hardware consists of several layers shown in the figure below. Several IO modules are used. The voltage and the current are sampled respectively by the Ni9225 and the Ni9246. Both can measure real-life voltages and currents which makes it easier to use in a calibration setting. The Ni9402 is used for the various synchronization signals. Finally, the Ni9269 is used to generate the signals needed for the validation of the reference MU.

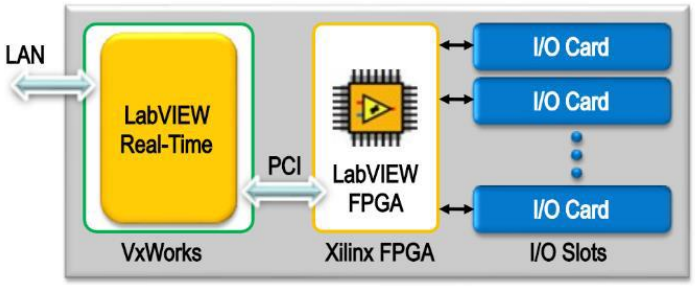

Figure: Schematic showing the different layers in the hardware.

The chassis has embedded in it one processor and a FPGA. Both are used in the merging unit. The FPGA is programmed to generate all necessary timing signals and oversees the sampling process of all voltage and current channels. Also, the FPGA resamples the signals to the proper speed as needed for the IEC61850-9 sampled value. The processor operates a real-time operating system and handles all network related tasks. The complete device can operate on its own and can act as a real MU. Which makes it less complicated to compare SV streams.

Finally, the PPS generated by the reference MU is a LVTTL signal and needs to be converted to be able to connect it with other MU's. The 1 PPS pulse must be converted to a fiber optic signal. This is done with a BNC to FO converter. The final calibration results with a demanding calibration procedure show that the total uncertainty for the absolute phase of the presented measuring system is in the order of 62 ns *k=2*.

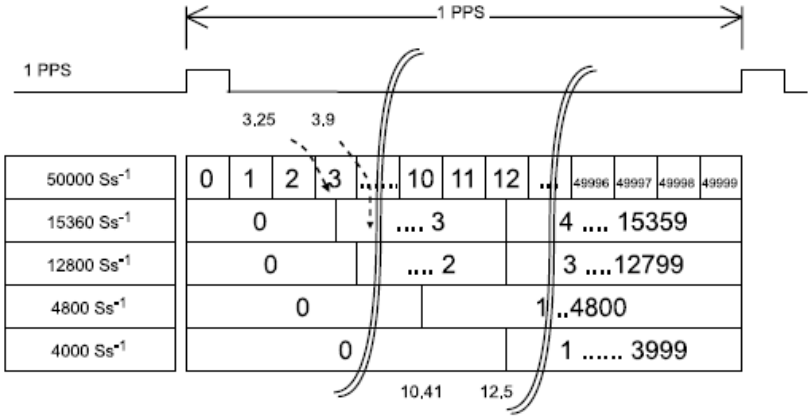

Figure: Scheme showing all resampling ratios needed. These are implemented in the FPGA.

SUN developed a low-cost implementation of a PMU. Reduced costs are a key for promoting the introduction of distributed digital power measurements. The widespread inclusion of Phasor Measurement Units (PMUs) as a core component in distributed power measurements is becoming increasingly important for the development of power system "smartness". However, PMUs with accuracy compliant to the standard Institute of Electrical and Electronics Engineers (IEEE) C37.118.1-2011 and its amendment IEEE Std C37.118.1a-2014 have typically costs that constitute a barrier to their introduction. A low-cost approach has been followed in the design of all the building blocks of this PMU. A key feature of the presented approach is that the data acquisition, data processing and data communication are integrated in a single low-cost microcontroller. Synchronization is obtained using a simple external Global Positioning System receiver, which does not provide a disciplined clock. The synchronization of sampling frequency, and thus of the measurement, to the Universal Time Coordinated, is obtained by means of a suitable signal processing technique. For this implementation, the Interpolated Discrete Fourier Transform has been used as the synchrophasor estimation algorithm. A thorough metrological characterization of the realized prototype in different test conditions proposed by the standards, using a high-performance PMU calibrator, is also shown.

In order to obtain an adequate level of accuracy and, at the same time, keep low the hardware cost, reference is made to the architecture reported in the next Figure below and only cheap components have been chosen. The input stages are constituted by low cost voltage and current transducers equipped with suitable analog

conditioning stages to adapt the signal level to the input range of the ADC. The core of the instrument is a low-cost Advanced Reduced Instruction Set Computer (RISC) Machine (ARM) microcontroller unit (MCU) with integrated ADC (analogue-to-digital converter) and Ethernet interface. It is responsible for the absolute time synchronization, data acquisition, signal processing and data communication. A key feature of the design is the lack of a GPSDO. Instead, a simple GPS receiver is used, and all the synchronization is derived by the PPS signal. Therefore, a suitable signal processing is adopted to obtain measurements synchronized to the UTC. Voltage and current synchrophasors, frequency and ROCOF are obtained by processing the synchronized signal samples through an Interpolated Discrete Fourier Transform (IpDFT) algorithm.

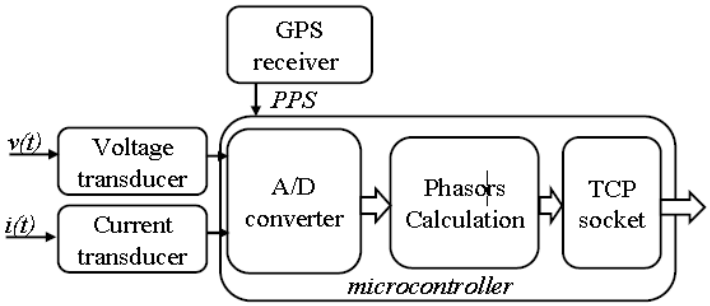

Figure: The proposed architecture for a low-cost Phasor Measurement Units (PMU).

Measurement data are communicated through a Transmission Control Protocol (TCP) socket to a host Personal Computer (PC); for the scope of this work, the standard Institute of Electrical and Electronics Engineers (IEEE) Std C37.118.2-2011 has not been considered. Results of the experimental tests are summarized in the Table for class P. They were obtained using an observation interval of four nominal 50 Hz cycles and a reporting rate of 50 fps , whereby the total execution time is only 7.8 ms for the two channels, i.e., quite lower than 20 ms, which is the time interval between two reporting instants. For sake of brevity, only results relative to voltage channel are presented; similar values have been obtained also for current channel.

Table: Maximum measured (Meas.) TVE, FE and RFE, and the corresponding limit values, in various testing conditions reported in IEEE Standards for Class P PMUs. The reported results refer to observation intervals of four nominal cycles and reporting rate of 50 fps.

Test Type	TVE max [%]		FE max [mHz]		RFE max [Hz/s]	
	Limit	Meas.	Limit	Meas.	Limit	Meas.
Frequency offset (±2 Hz)	1	0.11	5	1.0	0.4	0.13
Frequency offset (±2 Hz) +1% 2nd harmonic	1	0.19	5	4.7	0.4	0.19
Frequency offset (±2 Hz) +1% 3rd harmonic	1	0.15	5	1.1	0.4	0.15
Frequency ramp (±2 Hz at 1 Hz/s)	1	0.35	10	7.7	0.4	0.19
AM (10% at 2 Hz)	3	1.8	60	27.0	2.3	2.1
PM (0.1 rad at 2 Hz)	3	1.4	60	45.0	2.3	1.5

Conclusion

Overall, the conclusion of these achievements represents the finalisation of all aspects of Objective 2 by the project consortia, by providing references for the calibration of instruments with digital input or output, methods and devices, synchronization methods of sampling processes with various sampling rates and solution for distributed digital power measurements. This establishes in the whole the previously missing links for the existing analogue high voltage metrology infrastructure to the digital domain of time stamped sampled values.

Collaboration between partners relate to a common design and hardware setup that has been worked out between VTT and VSL for the reference SAMU as well as the distributed digitizer.

4.3 Objective 3

This objective was to develop **metrological tools** for the characterisation of devices that exploit sampled values in digital substations, such as **all-digital power and power quality meters** and **phasor measurement units (PMUs)**. This included e.g. studies on **limitations due to latency and computation time**, and characterisation of error sources in order to provide proposals for an **enhanced protocol for sampled values**.

Overview of the most remarkable results for this objective

First, to support metering applications based on SV, two platforms for receiving or sending the timestamped SV data stream were created. The first software platform was tested against two commercial devices to demonstrate their functionality. For more time critical applications, where seamless streaming from and to SV based equipment is required, a microcontroller-based SV-Generator and an SV-Receiver were built up and successfully tested with two commercial SAMU's, two instrument transformer bridges and with a commercial digital energy meter. The required software functionality for waveform generation and power meter algorithms was developed. The second software platform makes use of the existing 61850-9-2:2011 sampled value protocol as well as the enhanced new protocol 61869-9:2016 for higher sampling rates of 14.4kS/s in 50 Hz systems. Furthermore, effects on accuracy of electrical power and energy were simulated for different types of ADCs, number of bits, noise and jitter. Using this platform, an all-digital power and energy meter has been finally tested for the first time in Europe.

Second, for the PMU related aspect, a particular PMU algorithm has been identified and implemented for use with the SV protocol. It enabled to determine the time-critical performance of accurate measurements with respect to the PMU reporting latency. An open-source library for measuring PMU reporting latency was published and an extension to a Real Time Digital Simulator (64 PMU data streams) was developed. An integrated (Stand Alone Merging Unit) with Phasor Measurement Unit (PMU) functionality has been built and tested, implementing SV based on IEC 61869-9. The synchrophasor estimation algorithm has been optimized for computation performance to minimize delays as well as performance requirements in terms of CPU and RAM. This device is the first one in Europe, that is ready for commercial use. A further development has taken advantage of the SV extraction feature. A simple and new differential protection algorithm was developed and compared it with strategies involving commercial PMUs and relays. The system was implemented by performing the FFT from two different grid points and applying a fault criterium following the typical configuration of 87-L relays allowing its comparison with the other strategies. The developed new SV algorithm showed better tripping time than the PMU solution and is near to the tripping time of conventional solutions.

A data compression method for the SV protocol was enhanced and tested under real world conditions. The software package was made publicly available. It was designed for streaming raw measurement data, similar to the IEC 61850-9-2 Sampled Value protocol and to support high sample rate continuous point on wave (CPOW) voltage and current data and supported other measurement types. The developed data compression is lossless.

Several paper on the findings of the objective-related work have been published – see reference section.

Metrological tools for all-digital power and energy meters

Typical SAMUs do not perform power and energy measurements. They can include them, but they are not standardized yet. To this purpose a custom SAMU was developed by UNIBO. The SAMU is capable of power and energy measurements. Such measurements have been compared with reference power/energy meters. With this system, the link between traditional analogue power and energy metering and metering based on digital SV is closed. The new SAMU consists of (i) an OPAL simulator, being the processing unit of the SAMU; (ii) a resistive divider for the voltage input; and (iii) a shunt-plus-amplifier system for the current input. The developed SAMU accepts both IT and LPITs inputs (either analogue or digital); in particular, the $100/\sqrt{3}$ voltage level and $3.25/\sqrt{3}$, respectively (in the latter case, there is no need for a voltage divider). As for the current inputs, again, the SAMU accepts both the standardized input 1 A and 5 A for the legacy CTs, and the millivolt input signals from the current LPITs. Finally, OPAL features an IEC 61850-9-2 communication tool that allows the conversion of the digital stream of acquired data into the standardized "packets" to be sent to a generic control room or receiver. In detail, the OP4510 RTS features an IEC 61850-9-2 LE protocol for digital output data. This protocol allows to retrieve 80 or 256 samples per cycle, corresponding to 4000 and 12,800 samples, respectively, at a rated power system frequency of 50 Hz. Using an external clock, the Sample Value (SV)

timings were synchronized with an external source, namely the Oregano board, which synchronized the protocol timings according to a specific standard

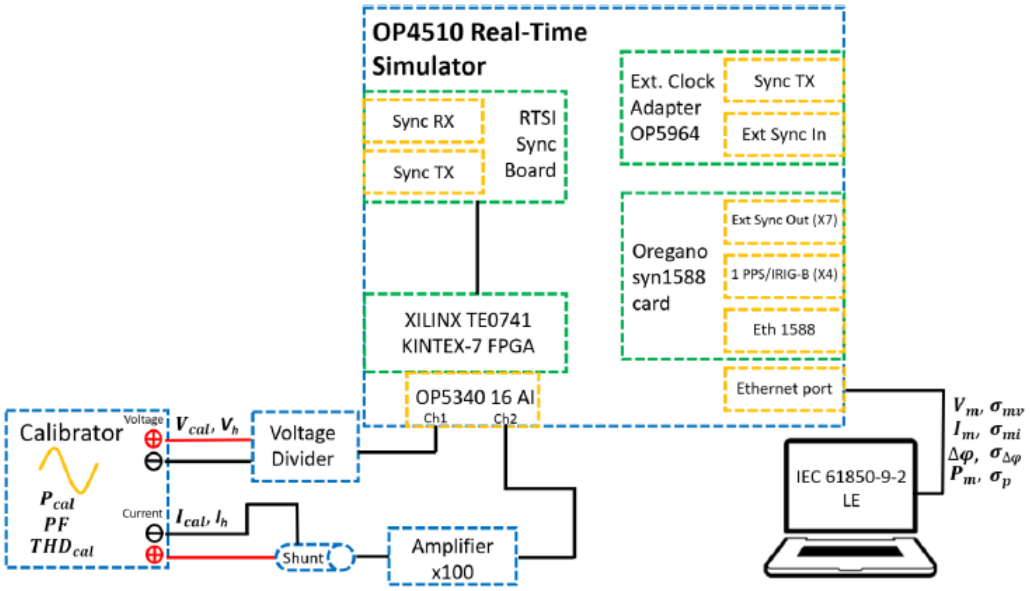

Figure: Final setup of the realized SAMU acquiring voltages and currents from the Fluke 6105A Calibrator and OPAL RTS, providing data using the IEC 61850-9-2 LE protocol.

By using the setup depicted in the figure above, 500 measurements of the following test were performed:

• Test at rated conditions. The voltage was set to 57 V and the current to 5 A (at 50 Hz).

• Test varying the amplitudes. From the combination of 80 %, 100 %, and 120 % of the rated voltage and 5 %, 20 %, and 10 0% of the rated current, 9 power values were applied and measured (always at 50 Hz).

• Test varying the power factor (PF). At rated voltage and current, the PF was set, varying from 1.0 to 0.1 at 0.1 steps.

Table: Power measurements at 120 %, 100 % and 80 % of the rated voltage, and at 100 %, 20 % and 5 % of the rated current at unitary power factor (PF).

V_{cal} [V]	I_{cal} [A]	P_{cal} [W]	P_m [W]	σ_p [W]	ε_p [%]	$\sigma_{\varepsilon p}$ [%]
	5.0	342	340.6628	$7 \cdot 10^{-4}$	0.3910	$2 \cdot 10^{-4}$
68.4	1.0	68.4	68.1076	$4 \cdot 10^{-4}$	0.4275	$5 \cdot 10^{-4}$
	0.250	17.1	16.9868	$2 \cdot 10^{-4}$	0.662	$1 \cdot 10^{-3}$
	5.0	285	283.9594	$2 \cdot 10^{-4}$	0.36511	$8 \cdot 10^{-5}$
57	1.0	57	56.7538	$3 \cdot 10^{-4}$	0.43199	$6 \cdot 10^{-5}$
	0.250	14.25	14.1513	$2 \cdot 10^{-4}$	0.692	$1 \cdot 10^{-3}$
	5.0	228	227.0986	$5 \cdot 10^{-4}$	0.3954	$2 \cdot 10^{-4}$
45.6	1.0	45.6	45.4130	$3 \cdot 10^{-4}$	0.4102	$6 \cdot 10^{-4}$
	0.250	11.4	11.3249	$1 \cdot 10^{-4}$	0.659	$1 \cdot 10^{-3}$

The results of these tests are listed in the Table. Overall, considering all the power measurements, the developed SAMU can be considered very accurate, even for the power measurements based on sampled values.

For digital energy meters based on SV, so far, no standards exist. For working out a reasonable test plan, PTB used the standard IEC 62053-22 about static meters for active energy (class 0.2 S and 0.5 S). It is consideration as the source for a test plan and for the accuracy requirements of a digital energy meter. Based on this standard, the measurements for the digital energy meter were divided into three parts: multi-phase digital energy meters with symmetrical loading, multi-phase digital energy meters with single-phase loading, but symmetrical multi-phase voltage on the voltage paths and influencing values. The measurement setup for the calibration of the digital energy meter is shown in the Figure below. The digital energy meter was measured

by using a self-built SV-generator (SV: Sampled value) with its corresponding LabVIEW-based program (marked as a blue block). There are three methods to measure the energy of the digital energy meter (marked as orange blocks): i) read the energy values from the display, ii) measure the number of the LED impulse or iii) measure the period of the LED impulse.

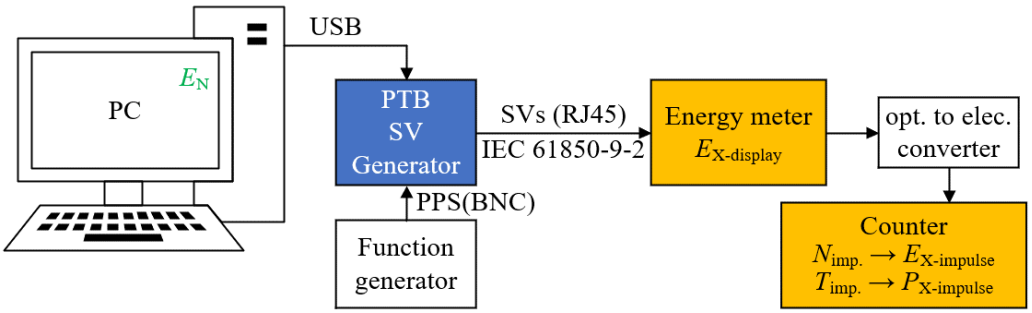

Figure: Measurement setup for the calibration of the digital energy meter

The SV generator box was considered as a substitute for the devices with the digital output (e.g., a Stand Alone Merging Unit (SAMU)) and can be used for the validation of an SV-based measuring device (e.g., for digital energy meters) without any numerical loss. The developed SV generator box (shown in the figure below) sends pre-programmed SV data over ethernet using the IEC 61850-9-2 protocol. The basic module is a 32-bit ARM Cortex-M4 CPU with ethernet and USB port. The SV data is programmed by the corresponding program using the USB connection.

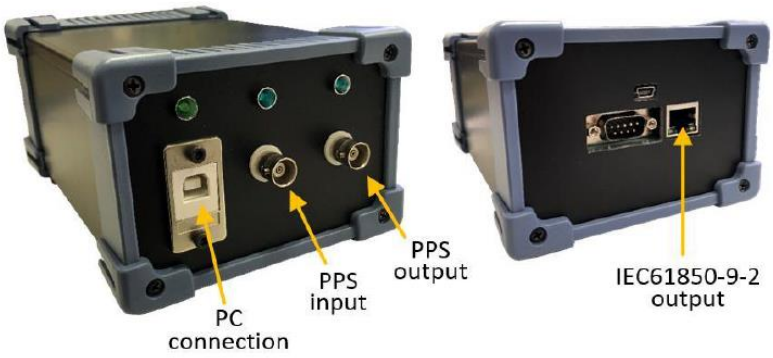

Figure: Photo of the SV-generator box

The corresponding program of the SV-generator box is mainly made up of three main functions: the SV waveform generation, the measuring functions and the power und energy calculation. The SV waveform generation function can generate three-phase four-wire current and voltage signals at the same time. The programmed currents and voltages and the phase angles can be differently set by the user.

Corresponding to the SV generation, the received SVs of *L*1 from another, very similar looking, SV receiver box are shown in the Figure below. The diagram shows that the SV receiver box received the repeated one-period signal ($t > 0.02$ s) from the SV generator box. Moreover, the differences between the sent and received SVs equalled to zero. This means that the SV receiver box receives exactly what is sent to it. Eventually, similar results were obtained by *L*2, *L*3 and *L*N as well.

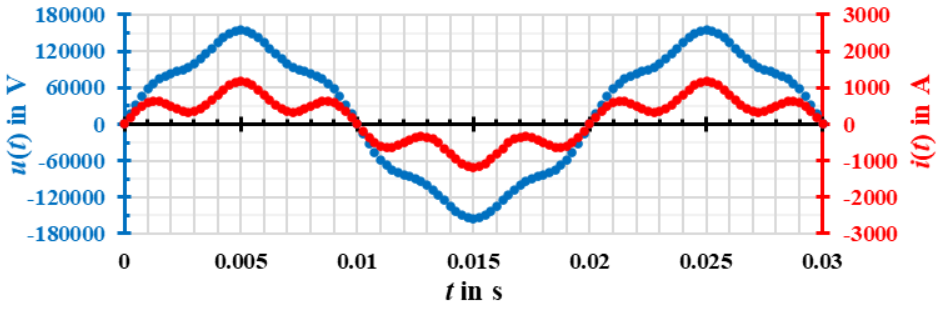

Figure: The received sampled values of voltage and current (*L*1) with the SV receiver box in the time domain. Some distortion has been added in the programmed SV data.

Finally, a commercial digital energy meter has been tested. It has the following main features:

Type:	L&G E880
Frequency:	50 Hz
Rated voltage UP:	100 kV
Rated current IP:	1000 A
Optic active energy output	R_A = 0.1 imp / kWh
Optic reactive energy output	R_R = 0.1 imp / kvarh
Accuracy class	Cl. 0.2S for active energy Cl. 1S for reactive energy

It has been shown with several measurements according to the test plan, that the calibrated error of the energy meter for the quantity "Energy" is far below its error class. Furthermore, other test results of the active energy by different readout methods are presented in the following table. Display readout ε_1; LED impulse counting ε_2; LED impulse period ε_3; LED impulse interval ε_4)

Table: Calibration results of the active energy by LED impulse.

No.	ε_1 in %	ε_2 in %	ε_3 in %	ε_4 in %
#1	0.00%	0.00%	0.015%	-0.012%
#2	0.01%	0.01%	-0.009%	-0.010%
#3	0.00%	0.00	-0.003%	0.018%

#1: I = 120 A, current phase = 0; U = 100 kV, symmetrical loading; PF = 1; t_s = 1000 s.

#2: I = 120 A, current phase = 0; U = 100 kV, symmetrical loading; PF = 1; t_s = 7200 s.

#3: I = 120 A, current phase = 0; U = 100 kV, symmetrical loading; PF = 0.8; t_s = 1250 s

Metrological tools for phasor measurement units

The Sampled Value PMU, developed by METAS, relies on a NI cRIO-9068 (National Instruments, Austin, US-TX), i.e. an embedded industrial controller equipped with a Linux Real-Time (RT) Operative System (OS) and a re-configurable Field Programmable Gate Array (FPGA) board. More precisely, the cRIO-9068 relies on a 667-MHz dual-core ARM Cortex-A9 (Arm Holdings, Cambridge, GBR) processor, and a Xilinx Artix-7 (Xilinx, San Jose, US-CA) FPGA board. In principle, the RT controller is responsible for capturing the SV data stream, whereas the second one can be used to expedite the processing of the current and voltage measurements. For this analysis, the cRIO-9068 has been programmed in LabVIEW 2020 Real-Time, with the addition of Shared Object libraries, specifically developed for the Linux RT OS (further details in Section III).

As shown in the Figure below, the cRIO-9068 is equipped with two independent Ethernet boards, compatible with the IEEE Std 802.3 (Gigabit Ethernet) and characterized by a communication rate of 100 Mbps (if auto-negotiated, up to 1000 Mbps). The fist board (Ethernet 0) is reserved for the bidirectional communication with the host computer and allows for programming the controller and retrieving in real-time the measurement results. The second board (Ethernet 1), instead, is responsible of capturing the SV data stream. The Ethernet transceivers communicate with the RT by means of a Reduced Gigabit Media-Independent Interface (RGMII). Once received the SV messages, the RT extracts the ASDUs, stores the current and voltage measurements, and processes them in order to extract the parameters of interest. In this sense, it is worth noting that the volatile and non-volatile memory are limited to 512 MB of Double Data Rate 3 Synchronous Dynamic Random-Access Memory, and 1 GB of NAND flash drive. For the characterization of the SV-PMU, the measurement setup in Figure below has been employed. A Meinberg LANTIME M600 Time Server (Meinberg Funkuhren, Bad Pyrmont, DEU) provides the time reference in terms of a Pulse-Per-Second signal that is aligned with UTC-CH by means of PTP synchronization protocol. A NI PXIe 1062Q hosts the IEC Std calibrator that consists of three main units:

• a synchronization board (NI PXI 6683) that is disciplined by the reference clock PPS and provides the trigger signals (PRS) for the other boards;

• a data acquisition board (NI PXI 4461) that generates the analog test waveforms (WRS) and re-acquires them (along with the PRS) for defining the reference values;

• an Ethernet interface module (NI PXI 8234) that is responsible for the communication with the SV-PMU and generates the SV data stream, synchronously with the analog output WRS signal.

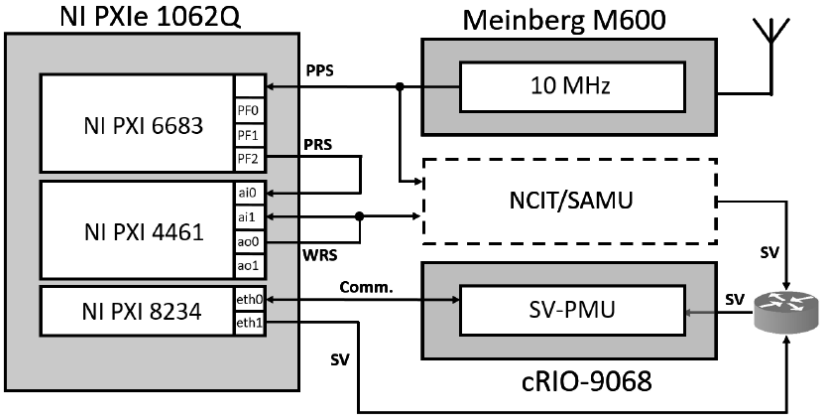

Figure: Measurement setup.

In the typical calibration setup, the device under test is represented by a NCIT or a SAMU that receives the analogue test waveform and converts it into an equivalent SV data stream. In this context, the SV-PMU can receive its digital input either from the IEC Std calibrator or the DUT. In order to characterize the SV-PMU performance, the IEC Std calibrator allows for a perfect knowledge of the SV data stream and facilitates the debugging process. Once validated the prototype, it will be possible to test it in real-world conditions, i.e. directly connected to a NCIT supplied with a known analogue input. The error parameters extracted from the SV-PMU prototype, i.e. TVE, FE and RFE, have been compared with same parameters, determined with the same number of ipDFT cycles (namely 5 cycles), extracted from a traditional PMU. Only a slight difference is noted when comparing the TVE (the analogue PMU presents lower values); while for the other two performances, the values appear to be almost the same.

A Stand Alone Merging Unit (SAMU) was built by COMSENSUS on top of a Phasor Measurement Unit (PMU) as depicted in the Figure below.

Figure: Design of integrated SAMU/PMU device

It is designed as a multifunctional metering and control electronic device that can be used for measuring voltage and current waveforms as well as observing and triggering digital statuses of the target systems. The high sampling data rate performed in time synchronized manner enables to follow highly dynamical phenomena on all voltage levels of the grid and extraction of measurements parameters such as synchrophasors, frequency, and rate-of-change-of-frequency. The device readily supports and is certified

according to the following standards: (i) IEEE C37.118 (for both M and P class accuracy), (ii) Parallel Redundancy Protocol (PRP) and High-availability Seamless Redundancy (HSR) redundant protocols for Ethernet-based data exchange, and (iii) GPS/Galileo, IEEE 1588 (PTP), and IRIG-B for time synchronization. The effort within the project was focused on the support of IEC 61850 for Sampled Values (SV) and Generic Object Oriented Substation Event (GOOSE) data exchange.

The synchrophasor estimation algorithm employed in the implementation is based on the three-point interpolated DFT algorithm utilizing the frequency calculated from a zero-crossing algorithm. The high-level functional diagram is depicted in the next Figure below. The advantage of the approach described towards the classical FFT based techniques is that it enables shorter input windows (w) for frequency estimation. A shorter window means a higher temporal resolution of a variable under consideration. Furthermore, the zero-crossing algorithm for frequency detection is straightforward to implement and does not need high computation power compared to pure FFT based methods. Moreover, in FFT based methods, only output filters are considered in our case we have two-stage filtering, one at the input and another at the output, giving us more room to filter out some dynamics that would negatively affect algorithms. Output filters are standard decimation algorithms with the same functionality as defined in the IEEE C37.118 standard. This kind of configuration enables to easily implement different filters if some more dynamics is needed in the output, e.g. for observing faults with higher dynamics. Since this is a software implementation, we can create additional parallel channels where some different non-linear filters can be tested in parallel with IEEE C37.118 compliant synchrophasor algorithms.

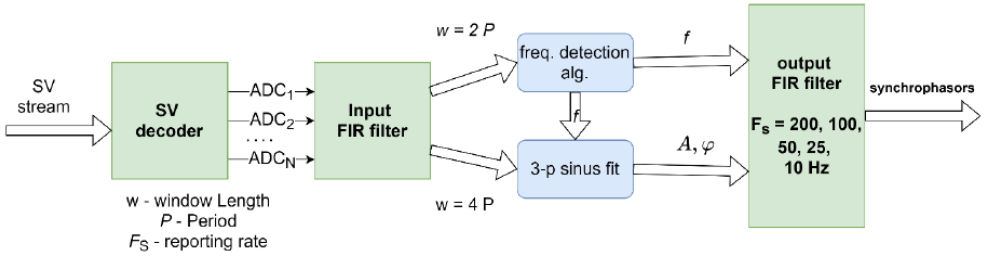

Figure: Block scheme of PMU algorithm

Further work by STRATH and Synaptec was related to the suitability of compliant PMU algorithms from the conventional analogue-based approach of the IEEE C37.118.1-2011 and the IEEE C37.118.1a-2014, for use with the IEC 61850-9-2 SV data as an input, rather than the conventional approach of using analogue inputs directly integrated within the PMU.

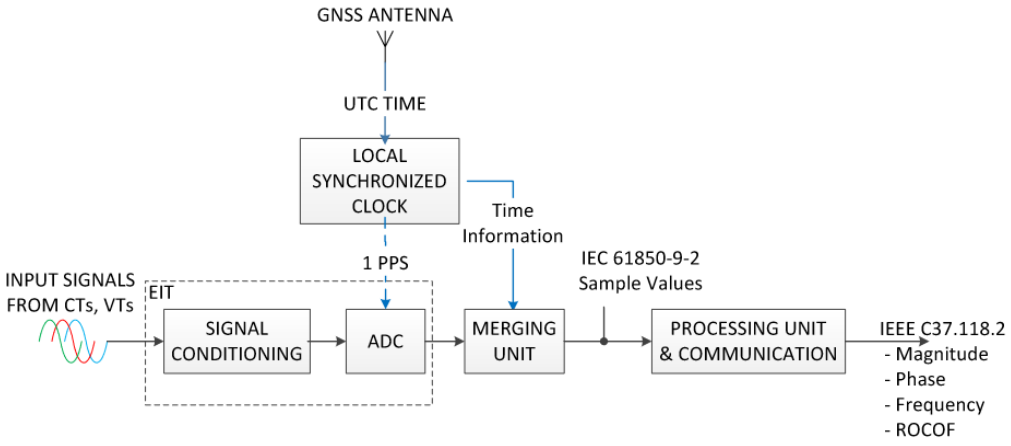

Figure: Block diagram of a PMU with SV data as input, according to IEC/IEEE 60255-118-1:2018, Annex E

In particular, it is important to assess the impact on measurement performance (if any) and on the delivery of data for real-time applications. In summary, it has been found that PMU algorithms based on the Enhanced Interpolated-Modulated Sliding DFT (E-IpMSDFT), demodulation and filtering, and Taylor-Fourier methods are immediately suitable for use with SV data, with little impact on real-time performance. Other algorithms typically

operate on large windows of data in batches, rather than performing processing on a sample-by-sample basis; therefore, these algorithms will likely result in large and variable PMU latency.

Another part of the work is related to a new method, developed to measure the reporting latency of a PMU very accurately and conveniently. The approach in this new method can also assess the impact on latency from using IEC 61850-9-2 SV data as the input to a PMU, compared to conventional PMUs with analogue inputs. The PMU algorithm processing occurs in a ‘‘soft real-time’’ manner; this is the cause of the relatively high standard deviation of latency, compared to the RTDS GTNET PMU, given in the Table. Due to adaptive filtering, which is unique to this implementation, the PMU reporting latency depends on the measured frequency value. The impact of this is shown through the tests at off-nominal frequency for the M class implementation in the Table, where the reporting latency decreases as the system frequency increases (due to the reduced window length).

In summary, the use of SV as the input to a PMU adds to the overall reporting latency due the additional stage involving a Merging Unit digitizing and packetizing the waveform data (approximately 800 µs for the Merging Unit under test). However, this value is dependent on the Merging Unit implementation, performance, and the number of waveform samples encoded per SV packet.

TABLE: Measured PMU reporting latency for various configurations: clocking configurations, PMU class, reporting rate, and signal input frequency

PMU device	PMU input type	Signal input	Configuration option (see Fig. 4 and Table 1)	Reporting rate, F_s (Hz)	PMU class	Mean latency (ms)	Max latency (ms)	Std. dev. of latency (μs)	Theoretical latency, based on window length (ms)	Difference between measured mean latency and theoretical latency (ms)
RTDS GTNET	Digital	50 Hz	2a	50	P	21.595	21.626	8.7	20.0	1.595
RTDS GTNET	Digital	50 Hz	2a	50	M	91.846	91.871	8.0	88.75	3.096
RTDS GTNET	Digital	50 Hz	2a	100	P	21.594	21.619	6.4	20.0	1.594
RTDS GTNET	Digital	50 Hz	2a	100	M	44.344	44.373	6.4	41.25	3.094
Adaptive Filter	Analogue	50 Hz	1a	50	P	20.234	20.285	28.9	20.0	0.234
Adaptive Filter	Analogue	50 Hz	1a	50	M	100.231	100.286	29.3	100.0	0.231
Adaptive Filter	Analogue	50 Hz	1a	100	P	20.240	20.286	27.6	20.0	0.240
Adaptive Filter	Analogue	50 Hz	1a	100	M	60.230	60.284	32.4	60.0	0.230
Adaptive Filter	IEC 61850 SV	50 Hz	2b (PMU does not require synchronization)	50	M	101.001	101.055	29.6	100.0	1.001
Adaptive Filter	Analogue	55 Hz	1a	100	M	54.780	54.830	31.8	54.545	0.234
Adaptive Filter	Analogue	45 Hz	1a	100	M	66.898	66.950	24.9	66.667	0.232

Limitations due to latency and computation time and data compression for enhanced protocol for sampled values

SUN examined the effects of resolution, noise and timestamps of sampled values on measurement results and on the accuracy of digital energy / power meters using experimentation and simulations. This section describes the configuration of the measurement, the synchronization system and the results of the impact on the digital power meter in different conditions, as well as the impact on the metrological performance of the power measurement when the current and voltage channels use different architectures for Analog-to-Digital Converter (ADC) and a different sampling clock.

This section has two subsections. The first section examines the accuracy of power measurement when the current and voltage channels have an ADC with different numbers of bits, different signal-to-noise ratio (SNR) and different jitter on the sampling clock. The second section examines the accuracy of power measurement when the current and voltage channels have a different ADC architecture and the same or different sampling frequency. The results presented in the first section have been simulated in MatLab environment. The results presented in the second section are experimental results obtained with LabVIEW by emulating a power meter, using ADCs with Successive Approximation Register (SAR) and Delta/Sigma (Δ/Σ) architectures.

A) Effect of bit number, noise and jitter

This section examines the accuracy of power measurement using a Matlab simulation in the following conditions: ADC on voltage channel with bit number: 12 and 24; SNR: 40 and 140 dB; no jitter on sampling clock. ADC on current channel with bit number: 12, 16, 20 and 24; SNR: 40, 60, 100 and 140 dB; jitter on sampling clock: 10 ns, 500 ns and 10 µs.

A Matlab function was developed for three features: waveform generation with White Gaussian noise (to simulate the SNR), ADC simulator with different number of bit, power meter simulator for measuring power in sinusoidal conditions. The power meter simulator extracts the active power, the reactive power, the apparent power and the power factor from the voltage and current waveforms, which was generated with the sampling clock at 4 kHz, after the quantization using the ADC simulator. The reference condition is represented by power in ideal conditions, that is sinusoidal waveforms with frequency of 50 Hz, root mean square (rms) amplitudes of 1 V and 1 A, with power factor equal to cos(π/4). It can be shown from all simulations, that SNR has practically no effect: all results corresponding to different SNR values are very similar.

The number of bits presents an effect only in the presence of a low jitter (10 ns), whereas in all other cases the resulting curves are practically flat. Differently from the resolution (number of bits) and noise (SNR) parameters, the jitter could remarkably worsen the accuracy in the power measurement, both in terms of its mean value as well as in the standard deviation of the measured deviations. Obviously, the worst condition is when the jitter is 10 µs on both the channels, here the maximum values of the errors, including the standard deviation are about 0.07 %, 0.04 % and 0.07 % respectively for active power, apparent power and reactive power.

B) Effect of ADC architecture and sampling frequency

In order to investigate the effect of different ADC and different sampling clocks, a measurement setup has been developed, based on a National Instruments (NI) PCI eXtension for Instrumentation (PXI) system.

A time base reference (10 MHz) was exported from Power Standard and given to the PXI system. Two clock sources use this time base reference to generate two sampling clocks for the voltage and current ADCs. A digital power meter uses the signals converted by the ADCs and extracts active power, apparent power and reactive power according to equations (3.1) - (3.5). These quantities are compared with the reference quantities retrieved from the Power Standard. The power standard is the Fluke 6105A (up to 1000V and 50A, 50 p.p.m. best accuracy), the clock sources are two NI PXI-5421 (16 bit, ± 12 V, max sampling frequency 100 MHz, variable gain) and the current shunt is Fluke A40B 5/0.8 A/V.

The following tests were performed: i) the same ADC architecture with the same sampling clock (sampling clock time base in the case of Δ/Σ); ii) the same ADC architecture with different sampling clock with difference at 1ppm, 10ppm and 100ppm (in the case of Δ/Σ, different sampling clock time bases resulting in the same differences in sampling clocks); iii) different ADC architecture with different sampling clock or sampling clock time base. The Table below shows the apparent power error, active power error and reactive power error in synchronized case with three configurations of ADC architecture, respectively, SAR-SAR, SAR- Δ/Σ and Δ/Σ − Δ/Σ.

Table: Apparent power error, Active power error and Reactive power error with same sample clock or time base in SAR-SAR, SAR- $\Delta\Sigma$ and $\Delta\Sigma$- $\Delta\Sigma$ configurations.

Configurations	ε_S [%]		ε_P [%]		ε_Q [%]	
	Mean	Std	Mean	Std	Mean	Std
SAR-SAR	-0.08	0.15	-0.09	0.19	-0.07	0.23
SAR-Δ/Σ	-0.05	0.15	36.30	0.21	-62.56	0.21
Δ/Σ–Δ/Σ	0.0117	0.0012	0.010	0.020	0.013	0.021

As can be seen from this Table, the worst case is the SAR- Δ/Σ configuration. Regarding the apparent power error, the average value is similar for each configuration, but the active power error and reactive power error reveal a different average value, which can be due to the internal architecture of the Δ/Σ ADC, that introduces a delay between the sampling starts with a consequent phase shift. This effect is present also in Δ/Σ − Δ/Σ configuration, but it is negligible because the delay between first rising edge of clock and the actual start of acquisition is similar for both ADC converters.

A data compression method for the SV protocol was enhanced and tested by Synaptec under real world conditions. It has been shown that a SV protocol with 4 kHz sampling rate produces 61 terabytes of data every year and with 14.4 kHz, what is the currently preferred sampling rate according to IEC 61869-9, it produces 218 terabytes of data every year.

Table: Specifications of the compression method comparing the obtainable size reduction (left) and computational load for the time to encoding (right)

Sampling rate (Hz)	Samples per message	Message size (bytes)	Size
4000	10	210	16.4%
4000	4000	46250	9%
14400	6	134	17.4%
14400	14400	97083	5.3%
150000	150000	431339	2.2%

Data storage method	Sampling rate (Hz)	Samples per message	Message size	Size	Time to encode
Raw data	14400	144000	10.3 MB	56.2%	423 ms
New method	**14400**	**144000**	**2.5 MB**	**13.5%**	**41 ms**
CSV	14400	144000	13.3 MB	72.4%	616 ms
CSV (+gzip)	14400	144000	4.2 MB	22.9%	602 ms

A software library with all routines was made publicly available. It is designed for streaming raw measurement data, similar to the IEC 61850-9-2 Sampled Value protocol whilst supporting high sample rate continuous point on wave (CPOW) voltage and current data as well as other measurement types. The developed data compression is lossless.

Conclusion

Overall, the targeted tools for the characterisation of devices exploiting sampled values in digital substations have been successfully created. It covered i) the tools for all-digital power and energy meters; ii) tools for all-digital phasor measurement units and iii) Studies on limitations due to latency and computation time with SV based measurements and providing a data compression method for enhancing the protocol for sampled values. As such, Objective 3 was achieved completely by the project partners.

The very close academia-industry cooperation between STRATH and SYNAPTEC led to excellent results that could not be achieved from a single partner.

4.4 Objective 4

Objective 4 is to develop traceable reference standards for the **verification of time and synchronisation methods**. This included study on techniques and algorithms such as PTP and White Rabbit for the synchronisation of sampling to a common time reference, both within and between digital substations. In addition, to carry out studies on **secure protocols for time dissemination**. To develop and validate **satellite-independent PMU** utilising distributed sensors.

Overview of the most remarkable results for this objective

Firstly, over the course of the project, PTB continued its established work on security for the Network Time Protocol (NTP) in the Internet Engineering Task Force (IETF). This culminated in the publication of the Network Time Security (NTS) standard as RFC 8915, which marked the first time that users could use NTP in a secured

(authenticated) fashion that was both reliable and scaled well (a server can serve large numbers of clients). While the accuracy here is not in line with the goals for smart grids, secure NTP can still be a valuable control tool for other synchronization.

Based on the experience gathered from NTP related work, PTB conducted research on security and self-assessment measures for PTP. Results were constantly transferred to the IEEE 1588 WG developing and maintaining the PTP standard, to facilitate improved PTP security. Some of this input was reflected in version 2.1 of the PTP standard (IEEE 1588-2019), which details about 20 main changes, three of which were related to PTB's input to the working group: adding security data, options for monitoring, and a high-accuracy profile oriented on White Rabbit. Transferability of PTP security methods to White Rabbit was found to be high.

Further, work on satellite-independent PMU measurement using distributed photonic sensors was completed. A synchromerger was finished, intended for up to 50 distributed photonic measurement devices over a 50 km radius. The PMU algorithm can be executed externally (cloud-based) using SV measurements or can be executed directly on the measurement device for real-time applications. This yielded a completely new technology for conducting wide area monitoring measurements without the need of time transfer to remote locations. The proof-of-concept setup was operated by a central interrogation unit, which by necessity required a calibrated time link. However, the far ends consisted of passive fiber links, with distances up to and beyond 30 km. This way, a measurement system covering a geographically significant area could be established, with only modest requirements for timing infrastructure.

In the Good Practice Guide, which is made available the FGII community at ZENODO, associated to this objective a collected overview was presented on how to assess both the accuracy and reliability levels and relate them to the required effort, for different digital methods of synchronizing clocks (such as PTP and White Rabbit, but also NTP or GNSS). The novel presented process enabled end users to judge the three aspects for (existing or future) possible technologies used to realize required time synchronization, all illustrated with numerous examples.

Several paper on the findings of the objective-related work have been published – see reference section.

Security and Reliability Work

Over the course of the project, PTB has continued its established work on security for the Network Time Protocol (NTP) in the Internet Engineering Task Force (IETF). This has culminated in the publication of the Network Time Security (NTS) standard as RFC 8915. While NTP is of secondary importance regarding the goals for smart grid devices due to its only millisecond-level to tens-of-microseconds-level accuracy, the work still relates to the project goals: NTP can still be used as a control mechanism, to ensure that no large synchronization errors occur, and the techniques for securing it are at least partly transferable.

Based on the experience gathered from NTP related work, PTB has conducted research on security and self-assessment measures for PTP. Results have been constantly transferred to the IEEE 1588 WG developing and maintaining the PTP standard, to facilitate improved PTP security.

The transferability of published and currently envisioned PTP security mechanisms to White Rabbit has been researched. A final feedback round with White Rabbit experts has concluded that transferability is high, and the transfer is relatively simple: White Rabbit uses PTP messages as part of its synchronization procedures, and securing these with PTP security mechanisms is the full extent of reasonable security measures for White Rabbit.

Also, research and evaluation of different self-assessment techniques has been concluded for PTP and NTP. A setup based on Meinberg LANTIME 3000 devices for the evaluation of self-assessment via PTP was built up and data has been collected and evaluated at PTB. This setup is different from the one originally envisioned, since the two involved devices must remain in separate buildings. The best observed self-assessment technology is Meinberg's proprietary PTP monitoring via HPS-enabled PTP ports. Other options, standardized in PTP v2.1, have been evaluated and tested, but have been found slightly less ideal.

Some of this input is reflected in version 2.1 of the PTP standard (IEEE 1588-2019), which details about 20 main changes, three of which are related to PTB's input to the working group:

- *Options for greater security*: a new TLV is defined, in Section 16.14. for cryptographic message and source authentication. Additionally there is a new informative annex, Annex S, on security. The previous security approach, Annex K in the 2008 edition of the standard, has been removed. This certainly improves the capabilities of PTP in the spirit of our research results, although the definition of specific key establishment methods for the security procedures is left for future versions.

- *Options for monitoring*: options for monitoring PTP implementations are defined in 16.11 for Slave Event Monitoring and Annex M for Performance Monitoring Options.
- This is a step in the right direction from the point of view of our research, even though more direct monitoring through backwards synchronization (time source pretends to be time receiver and receives synchronization traffic from the actual time receiver to evaluate the quality of the synchronization) would be better still. Such techniques are to this date used only in proprietary PTP adaptations, but something like this might be suitable for a future version of the standard and the project partners will certainly recommend it.
- *New options and default profile for enhanced synchronization performance:* new options are defined in Section 16.7 for configurable correction of timestamps, in Section 16.8 for calculation of the delay Asymmetry for certain media, and Annex O for Layer-1 based synchronization performance enhancements. A new High Accuracy Delay Request-Response Default PTP Profile is defined in J.5. Related additional informative annexes were added: Annex P which explains how to implement the new profile to achieve sub-ns synchronization, and Annex Q which provides calibration procedures. These enhancements are based on White Rabbit.

  This means that transferring the security methods to White Rabbit is even more of a likely path to take in the future, since PTP and White Rabbit have become even more closely related.

Together, the mentioned activities represent extensive studies on secure protocols for time dissemination, with numerous usable results, as well as active facilitation of their take-up in two major protocols (NTP and PTP), as well as preparation for use in a third (White Rabbit). This fulfils the security-related aspects of Objective 4.

Distributed satellite-independent PMU

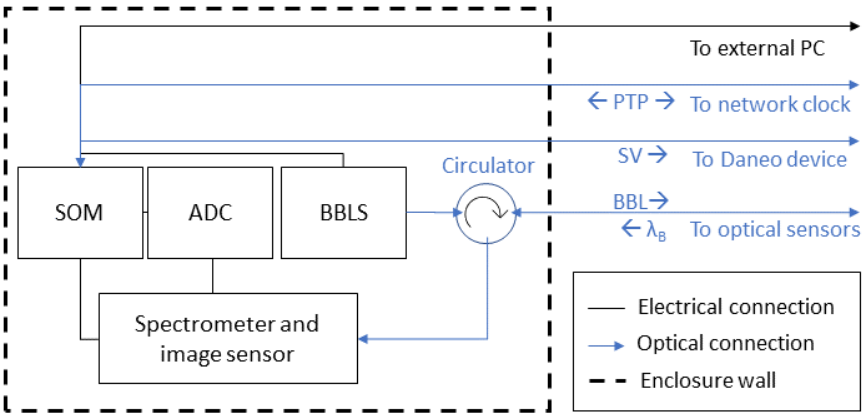

Figure: Interrogator block diagram fort he distributed PMU

Further, work by STRATH and Synaptec on satellite-independent PMU measurement using distributed photonic sensors has been completed. The synchromerger has been finished at Synaptec and is intended for up to 50 distributed photonic measurement devices over a 50 km radius. It is a product for satellite-independent PMU measurement using distributed photonic current sensors. The PMU algorithm can be executed externally (cloud-based) using SV measurements or can be executed directly on the measurement device for real-time applications. STRATH has contributed to firmware development, including retrospective time-stamping of distant measurements upon receipt at the central Synchromerger device. The system has been prototyped in the laboratory, with results reported to project partners.

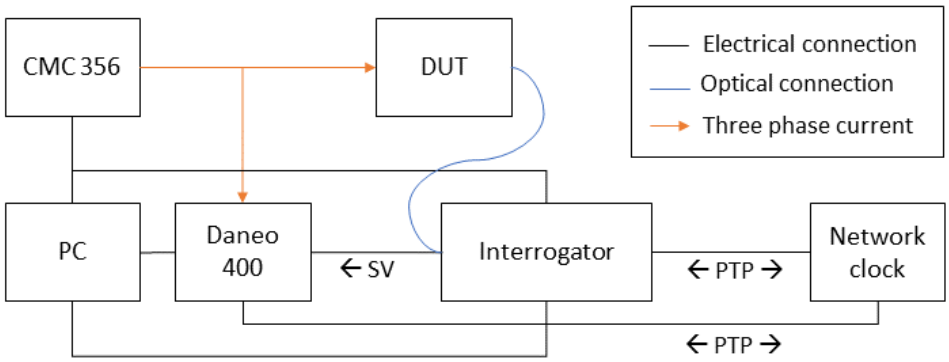

Figure: Calibration setup fort he distributed PMU

This yields a new technology for conducting wide area monitoring measurements without the need of time transfer to remote locations (e.g., via satellite). The proof-of-concept setup is operated by a central interrogation unit, which by necessity requires a calibrated time link. However, the far ends consist of passive fiber links, with distances up to and beyond 30 km. This way, a measurement system covering a geographically significant area can be established, with only modest requirements for timing infrastructure.

Satellite-independent Time Link Calibration and User-side Technology Assessment

PTB and VTT contributed to a joint paper, specifically describing pre-deployment assessment of time transfer technologies. It has been published online at EFTF 2021 and presents a collected overview on how to assess both the accuracy and reliability levels and relate them to the required effort, for different digital methods of synchronizing clocks (such as PTP and White Rabbit, but also NTP or GNSS). The presented process is intended for end users who require time synchronization but are not certain about how to judge at least one of the aspects. It can not only be used on existing technologies but should also be transferable to many future approaches. The paper further relates this approach to several examples, discussing in detail the approach of medium-range White Rabbit connections over dedicated fibers, a method that occupies an extreme corner in the evaluation, where the effort is exceedingly high, but also yields excellent accuracy and significant reliability.

Based on this and other material, PTB compiled the findings into the Good Practice Guide “Reviewing accuracy and security of digital time synchronization protocols”, which is made public available on the the FGII community at ZENODO – see reference section.

Furthermore, an existing mobile atomic clock has been used at PTB for in-laboratory, satellite independent calibration of time links required for project measurements. This includes a study at the PTB Braunschweig campus about the feasibility of calibrating several time sources using a transportable clock providing a 1PPS source. In this, the transportable Caesium atomic clock is first measured against a local timescale, after which it is transferred to a remote location, where the offset of a local 1PPS to the transportable clock is measured. This way, a time link of any length can be calibrated without having to determine the delay of the link itself.

Table: Individual steps of our comparison procedure

Step #	Description	Aim
1	Measure the mobile clock C over a long period against the used UTC(k) reference	To determine the rate of the mobile clock
2	Immediately before transport, determine the level difference, (1 PPS UTC(k) + K1) – (1 PPS C + K2) with the hardware (cables K1, K2, counters) selected for use in the target location	To determine the latest time offset of the mobile clock to the UTC(k) reference
3a, 3b, …	Evaluate different target sources Sa, Sb, … by measuring the differences (1 PPS Sa + K1) – (1 PPS C + K2)	To infer the difference of the target sources against the actual UTC(k) reference by proxy
4	After finishing the measurements, transport the mobile clock C back to the same UTC(k) reference used in step 1, and measure it against that again	To confirm that the transport of the mobile clock C has not negatively influenced its offset

The overall procedure was performed on PTB's Braunschweig campus, but is equally suitable in the context of electrical grids, for example in the calibration of substation time links. In that case, a similar mobile clock could be transported from the closest UTC(k) reference to the main time source used in a substation, transported back and the measurements used for confirmation of correction of the substation's offset.

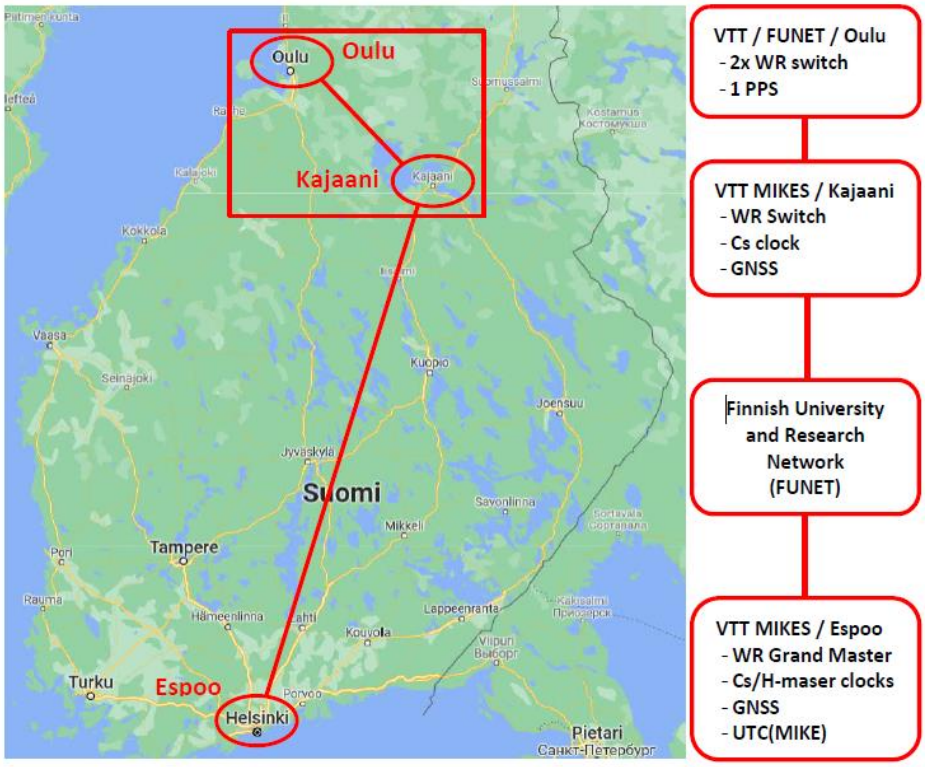

Figure: White Rabbit links between Espoo and Kajaani, and Kajaani and Oulu.

Next, a set of White Rabbit and PTP synchronisation devices have been verified and used at PTB, for distributed electrical measurements in the course of the project. VTT has been investigating calibration of time links by using GNSS-based methods, TWSTFT (Two-way satellite time and frequency transfer), PTPv2 (IEEE 1588-2008), White Rabbit PTP, and transportable Cs clocks. The work has been done in collaboration with a Nordic TSO for use in transmission grids. Methods and hardware for traceable references have been examined. Furthermore, VTT have been able to contribute their experience with long-range White Rabbit connections, including details and stability of a fiber-based time link being operated over a significant length of time. The White Rabbit link is built in Finland, with the far ends divided by a distance of 140 km.

Results from this relatively long link of White Rabbit time synchronization has been shown. A 225 km link or

shorter is what can be expected in a transmission grid. Link stability has been shown to be two orders of magnitude better then what is needed by PMU applications or IEC 61850 substations. But most importantly, the link is independent of any GNSS system, only relying on local national UTC realization and dissemination of frequency over a synchronous ethernet connection. Building dedicated WR networks for the transmission grid may be prohibitively expensive, but the modern society is in general more dependent on accurate time distribution not only for electricity grids, but also for e.g. telecom applications. More such synergies may be recognized in the future, easing the decision to invest in national timing infrastructure.

Future substations may rely on such time transfer technology, independent of any GNSS system. Or the time link may be used as one of the means of time or frequency distribution, providing added security from jamming and spoofing attacks on GNSS.

The sum of this activities satisfies those aspects of Objective 4 related to the development of satellite-independent traceable reference standards for the verification of time transfer links.

Conclusion

The combined expertise from PTB and VTT allowed to effectively cooperate for a joint paper. The work on satellite-independent PMU measurement using distributed photonic sensors was only made possible by the very close academia-industry cooperation between STRATH and SYNAPTEC.

Overall, work on the targeted traceable reference standards, satellite-independent time transfer, security methods and distributed PMU validation has been successfully finished. As such, Objective 4 was achieved completely by the project partners.

Further references of other open access publications from the project consortium:

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Ghaderi, A.; Mingotti, A.; Peretto, L.; Tinarelli, R. Low-Power Voltage Transformer Smart Frequency Modeling and Output Prediction up to 2.5 kHz, Using Sinc-Response Approach. Sensors 2020, 20, 4889. https://doi.org/10.3390/s20174889.

Mingotti, A.; Peretto, L.; Tinarelli, R. Toward the Standardization of Limits to Offset and Noise in Electronic Instrument Transformers. Sensors 2020, 20, 4061. https://doi.org/10.3390/s20144061.

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Sodin, D.; Rudež, U.; Mihelin, M.; Smolnikar, M.; Čampa, A. Advanced Edge-Cloud Computing Framework for Automated PMU-Based Fault Localization in Distribution Networks. Appl. Sci. 2021, 11, 3100. https://doi.org/10.3390/app11073100.

5 Impact

To ensure that the power systems scientific community benefited from these new or enhanced measurement capabilities, the following ways of disseminating project results were pursued:

- Peer reviewed open access scientific publications (39) some of which are highly cited
- Conference presentations or posters (33)
- Two stakeholder workshops were organised. The project members regularly reported to meetings of IEC TC 38 WG 47 to reach a wider audience and in particular the scientific community.

- Due to the projects partner structure, a close cooperation between the partners from universities and NMIs also supported the transfer of knowledge between the metrological and scientific community.
- The project published 7 datasets, five of these are datasets were required for publications, another one is a dataset of measured 3-phase medium voltage and current waveforms from a MV grid, and the last is a Software Library with a method for lossless compression of power system data.
- Two Good Practice guide have been compiled and made publicly available via the project's ZENODO community
- Articles published in a trade/professional press (11). One of them is not open access. Another is accepted for publication in the CIGRE ELECTRA #319 WG A3.31 Report on "Accuracy and Calibration of Instrument Transformers with Digital Output". The remaining articles are open access.

Impact on industrial and other user communities

The project has improved, and extended, electrical power and energy metrology infrastructure at the level of NMIs, universities, research centres and two SME's providing solutions for the control, protection, and monitoring of power networks. This covered calibration facilities for the instrumentation with SV (such as instrument transformers, SAMUs, energy meters and all-digital PMUs) and enhanced capabilities for time dissemination. The stakeholder committee included 29 members at the end of the project and has received regular newsletters. Stakeholder-supplied digital instrumentation has been successfully used for testing plausibility of project-developed measuring systems. Two industrial stakeholder workshops were held. At least 5 calibrations were carried out with respect to SAMU's, a digital energy meter and a high voltage digital instrument transformer. Associated companies were European companies. 5 follow-on collaborations with European companies were realised. One of this is a common IP exploitation on the development of commercial PMU/Merging Unit device.

Impact on the metrology and scientific communities

The project developed new and demanding measuring techniques and capabilities with claimed near future additions or extensions to CMC statements. Further knowledge dissemination to the metrology and scientific communities. The project and its objectives were presented in several meetings and workshops e.g. the Power and Energy Experts Meeting, Satellite Meeting CPEM 2018, and to a workshop of a transmission system operator.

Impact on relevant standards

This project generated results valuable to standardisation work within e.g. IEC, CENELEC and IETF/IEEE. Liaisons were accomplished by members of the project, who were active within the respective committees. The partners who were members of corresponding technical committees have been informing them about the results of this project and endeavouring to ensure they were incorporated in any updates to the standards.

- Workshops or informational meetings with standardisation bodies. The project, its activities and early research results were presented during several standards related meetings, e.g. IEC TC 38 and CENELEC TC 38. This led to more in-depth presentations and discussions with e.g. IEC TC38 / WG 47.
- Input to new or updated standard documents. Project partners actively participated in various concrete working groups in Standardisation Bodies by either face-to-face meetings or web meetings.
    - JWG 55 of IEC TC 38 "Uncertainty evaluation in the calibration of Instrument Transformers". The key output was the Technical Report IEC/IEEE TR 61869-105, which is now in the committee draft status. The forecasted publication date is November 2022. This stands as a common viewpoint of the evaluation of uncertainty in calibration and its application in testing procedures for ITs.
    - WG 47 of IEC TC 38 "Evolution of Instrument transformer requirements for the modern market". The partners worked on some preliminary documents relevant to uncertainty requirements of digital instrument transformers for PQ measurements and about the implementation of PMUs, which were circulated in IEC TC 38.
    - WG ntp of area "Internet" (int) of IETF "Network Time Protocol". Input to various drafts was given to the draft "draft-ietf-ntp-using-nts-for-ntp", which was made into a standards track RFC document in September of 2020. Project partners plan to continue to be involved in the WG, especially aiming at taking influence on the upcoming NTP version 5.

- Subcommittee “Security” of WG PNCS “Precise Networked Clock Synchronization” of IEEE. Input was given for revision 2.1 of the standard document P1588 “Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems”. Project partners continue to be involved in the WG, with a specific interest of White Rabbit security.
- Involvement in the activity of the IEC TC38 WG37 of the new IEC 61869-7 (Low Power Electronic Voltage Transformer) and IEC 61869-8 (Low Power Electronic Current Transformer) has led to tangible progression in the development of standards. Both Standards include Analog and Digital output of Low Power Instrument Transformers were already sent to TC38 Secretary for circulation and the IEC 61869-8 is now in the committee draft status. Both are forecasted for publication in December 2022. Project partners plan to continue to be involved in these activities.

Longer-term economic, social and environmental impacts

This project is supporting the transition of the grid from analogue to digital control, which may take decades as large-scale replacement of equipment is necessary. The use of such new next-generation ITs and PMUs in digital equipped substations is the prerequisite for successful integration of wide-scale connection of decentralised renewable energy sources in the high voltage distribution and transmission grid and for ensuring stability of the highly vulnerable European power grid under these increasingly complex and challenging conditions. The project facilitates this by providing test and calibration systems for these digital instrumentations. The project results are directly impacting the competitiveness of European industry in their endeavours on the international market for electricity supply, by providing them with the metrology tools to unambiguously prove the quality of their equipment. This quality is one of their prime selling arguments giving European industry a decisive global competitive advantage. To meet the requirements for a substantial impact in the long-term, the following project outputs provide benefits to industrial end-users and stakeholders:

- Many new or enhanced measurement capabilities are ready for digital or non-conventional instrument transformers, stand-alone merging units, digital energy and PQ meters as well as all-digital phasor measurement units by the NMIs, universities and research centres. This now largely support the procurement of new systems or components for the digital instrumentation in high-voltage substations. Target beneficiary groups are transmission and distribution system operators (TSO, DSO) and major equipment manufacturers.
- A metrological infrastructure for steady state and dynamic measurements on digital instrument transformers by providing proper calibration services including scheduled CMC submissions from three partners. Beneficiaries are manufacturers and purchasers of such equipment.
- Reference measuring systems for stand-alone merging units with time synchronisation by providing proper calibration services including scheduled CMC submissions from two partners. Further Test systems for digital energy and PQ meters are available from two partners. Target beneficiary groups are transmission and distribution system operators (TSO, DSO) and major equipment manufacturers.
- Improved standardisation by providing input or recommendations to several standards related to instrument transformer technology (IEC TC38) and related to time synchronization (IETF, IEEE)
- Improved knowledge and expertise in the European Metrology landscape in the field of testing new digital substation instrumentation technology.

6 List of publications

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