FINAL PUBLISHABLE REPORT

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Internal Funded Partners:	External Funded Partners:	Unfunded Partners:
1 LNE, France 2 BAM, Germany 3 CMI, Czech Republic 4 JV, Norway 5 NPL, United Kingdom 6 PTB, Germany	7 CNRS, France 8 SURREY, United Kingdom 9 ULiv, United Kingdom 10 ULILLE, France 11 UPC, Spain 12 UPEM, France	13 METAS, Switzerland
RMG: -		

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16ENG06 ADVENT

TABLE OF CONTENTS

1 Overview

The roll-out of 5th Generation (5G) telecommunications across Europe started in 2020. This coupled with the emergence of the Internet of Things (IoT) with its potentially 50 billion connected and continually operating electronic devices, will strongly increase the demand for energy leading to an associated need for more energy-efficient systems. This project has provided traceable measurements of power, losses and emerging electronic materials properties and the scientific knowledge required for the development of ultralow power devices. This is a significant contribution that will enable the European electronics industry to reliably develop more efficient power managements systems for next generation ultra-low power devices.

2 Need

The ongoing IoT and the future 5G radio access network will have a fundamental impact on the daily life of all European citizens. Sensors, the cornerstone of IoT, will be everywhere – in the car, the house, in industrial process monitoring etc. 5G communication systems will provide greater connectivity important in high speed Machine-to-Machine data exchanges with low time before response (latency). The high data-rate aspect of 5G at mmWave frequencies makes power consumption and thermal energy losses as heat very challenging to manage in wireless devices. The global greenhouse gases emissions in the Information and Communications Technology (ICT) sector has increased by half since 2013, rising from 2.5% to 3.7% of global emissions ("Lean ICT - Towards Digital Sobriety", The Shift Project, March 2019). Within this, 20 % of the footprint is attributed to personal mobile networks and mobile devices. Phones and tablets have produced the strongest percentage increase of greenhouse gas emissions in the ICT footprint.

Traceable and accurate data produced by innovative power sensors are needed to enable European mobile device manufacturers to improve their power management system efficiency and operating lifetime. This is particularly important for battery technologies used in smartphones and tablets. Multi-disciplinary metrology approaches proposed in this project will support the ICT sector's development of ultra-low power devices and therefore aids reduction of the European (and global) carbon footprint. The lower the power consumption of an electronic device, the longer it will continue functioning without recharging or changing the battery.

Improvement of the energy efficiency of devices and processes is therefore a key component for sustainable development of European products. Due to restrictions in current scaling strategies and dramatic thermal issues (particularly in wireless systems), semiconductor and electronics manufacturing roadmaps are aimed at the introduction of novel materials, more complete component characterisation and more efficient power management at the system level that will lead to the development of novel ultra-low power devices. To support industry in facing these challenging issues, traceable measurement techniques have been developed in this project to establish a robust metrology framework for in-situ, in-operando and multi-physics characterisation of advanced materials and components, and for reliable and accurate data for an efficient power management system.

3 Objectives

The overall objective was to achieve traceable and accurate measurements of the power consumed by ultra-low power and high frequency energy efficient electronic materials, devices and systems in order to support their development in both industrial and research sectors.

The specific objectives of the project are:

1. To develop nanometrology adapted to the in-situ and operando characterisation of advanced new materials proposed for the next generation of ultra-low power energy-efficient devices. These measurements will include impedance measurements (capacitance, resistance and inductance), piezo-electric/piezoresistive stress (200 MPa) and strain (0.02 %) responses to the application of electric (up to 4 MV/cm) and magnetic (up to 2 T) fields, as well as temperature and pressure in the range encountered in electronic devices.

2. To develop frequency and time-domain techniques for the simultaneous measurement of dynamic thermal profiles, electro-magnetic field sensing, DC electrical power consumption and RF operating waveforms for a wide range of RF electronic components (operating in-situ, under realistic conditions). These techniques to be combined with a multi-physics approach, which will establish rigorous energy budgets, and diagnostic capabilities, for a wide range of electronic components

(operating in-situ, under realistic conditions), required for next-generation communications. The uncertainty in the measurement of the power efficiency to be reduced to less than 1 %.

3. To develop embedded sensors and the associated calibration and measurement techniques to accurately measure power consumption of wireless systems (mobile phones, tablets and connected devices) and to improve the effectiveness of analogue and RF tests of components and systems. The power measurement techniques will be able to characterise and calibrate on-chip power sensors with an uncertainty of less than 10 µW.

4. To facilitate the take up of the technology and measurement infrastructure developed in the project by the measurement supply chain (accredited laboratories), standards developing organisations (ISO) and end users (the semiconductor industry, and the telecommunications sector).

4 Results

Objective 1: To Develop Nanometrology adapted to the in-situ and in-operando characterisation of advanced new materials proposed for the next generation of ultra-low power energy-efficient devices. These measurements will include impedance measurements (capacitance, resistance and inductance), piezo-electric/piezoresistive stress (200 MPa) and strain (0.02 %) responses to the application of electric (up to 4 MV/cm) and magnetic (up to 2 T) fields, as well as temperature and pressure in the range encountered in electronic devices.

The characterisation of novel materials, such as ferroelectric, multiferroic, and piezoelectric-resistive materials, requires a joint effort in improved impedance, material structure and compositional metrology. The impedance measurement at nanoscale suffers from a lack of traceability; stress and strain measurements as well as structural analysis of such materials do not enable the correlation of material structure and device functionality with enough resolution and reliability. Only in-situ electric field and strain have been measured with structural identification, and with polarisation depth dependence to approximately a μm depth resolution.

The new metrology capabilities at nanoscale needed for the characterisation of semiconductor devices and piezo materials strongly interests standardisation bodies as a source of content for future international standards. Development of metrology for static and dynamic force, electrical, magnetic and thermal property measurements are required to characterise ultra-low power devices based on piezo-electric/piezo-resistive materials.

In ADVENT, a metrology platform, required for characterising in-situ and in-operando advanced new materials, such as Piezoelectric and Ferroelectric materials, has been developed through three main but different approaches: impedance measurement based on Scanning Microwave Microscopy (SMM), analytical in-situ X-ray techniques (XRD, GIXRF-EXAFS), and mesoscale characterisation (TEM and IR-SNOM). These approaches required the development of sample preparation techniques that went beyond the state of the art.

Metrology platform – part 1: impedance measurements based on SMM

The development of material or devices requires the knowledge of properties such as permittivity or permeability and of specific electrical quantities such as the electrical capacitance. The impedance measurement gives access to this critical data that is of strong interest for industry keen to develop low power devices.

SMM is one possible approach for measuring impedance (capacitance, resistance and inductance) at nanoscale. The magnitude of measured capacitance, resistance and inductance may be down to the atto-farad, milli-ohm and pico-henry ranges, respectively.

SMM consists in a scanning probe microscope (SPM), e.g. an atomic force microscope (AFM) for LNE and METAS, interfaced with a vector network analyser (VNA) (**Figure 1**). While the conductive SMM tip scans over the sample surface, it irradiates microwave signal generated by VNA. The signal is partly reflected at the sample surface and a part travels through the tip to the VNA electrical connection. The ratio between the sent and collected signals, the so-called S_{11} scattering parameter, as recorded by VNA depends on the impedance of the measured local region of the sample. As a result, in addition to the topography data of probed regions, SMM is also capable of simultaneously mapping electrical properties of these areas. Compared to conventional characterisation techniques using microwave signals, the SMM technique allows users to perform electrical

characterisation of energy nanomaterials due to the extreme sharpness of the SMM tip (around tens of nanometers).

The issue in using such instrumentation is in its lack of traceability to the International System of Units (SI). One of the aspects of the ADVENT project was to develop impedance standards at nanoscale to establish traceability and to improve measurement accuracy, reproducibility and repeatability. This work represents very important challenges in different technical aspects. On one hand, the target uncertainty of capacitance measurements was ± 10% and capacitance standard values was targeted down to the attofarad range. On the other hand, the measurement of high values of piezoelectric material permittivity, based on capacitance measurements, is very challenging because of a non-linear behaviour (capacitance versus area), which makes the extraction of the electrical permittivity difficult. In ADVENT, first attempts for measuring piezoelectric devices have been realised by LNE and METAS.
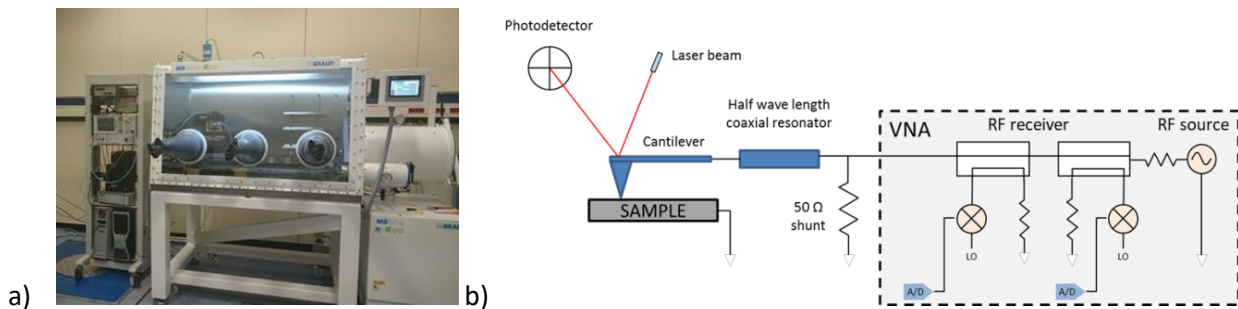

Figure 1: A photo of the LNE setup, where the SMM is located inside a glove box. b) Schematic diagram of the cantilever based SMM housed in LNE.

In ADVENT, different standards (capacitance values from attofarad to femtofarad, resistance values from milli-Ohm to kilo-Ohm, inductance values from picohenry to nanohenry) have been designed and manufactured by LNE and METAS (**Figure 2**). Regarding the capacitance standards, LNE has achieved the realisation of ultralow capacitance standards down to 13 attofarad corresponding to the project's targeted value. The sample characterisations performed at LNE and at METAS have been carried out through topographical, electrical and dimensional measurements.
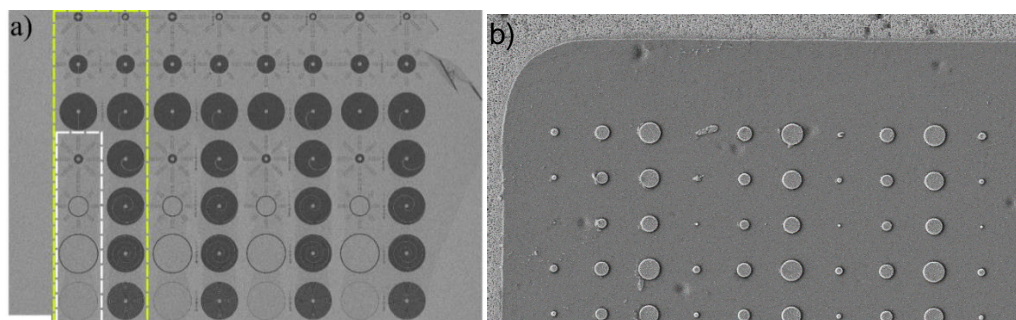

Figure 2: a- Large SEM image of capacitance, resistance and inductance standards developed by METAS. b- Large SEM image of ultralow capacitance standard developed by LNE.

METAS and LNE rely on a method, which is modified from the short-open-load (SOL) approach used to calibrate one-port VNA. To demonstrate the powerful capability of the SMM to calibrate capacitors at nanoscale with a guaranteed traceability to the SI, a substitution method was applied at LNE by performing capacitance measurements on two "unknown" samples. These were calibration kits from a French manufacturer (MC2-Technologies) which have the same number of patterns and capacitors and with similar configurations (four SiO_2 dielectric terraces of different thickness) to the reference sample but came from different growth batches and do not have the same Si substrate (different doping levels). The calibrations were performed at the VNA working frequency of 3.808 6 GHz and the SMM was calibrated using the selected capacitor triplet (C_1=8.57 fF, C_2=4.42 fF, C_3=0.18 fF).

The measured capacitance values have been found ranging from 0.1 fF to 3.1 fF (**Figure 3**) with a combined relative uncertainty that varies from 14 % to 5 % respectively. This corresponds to the 10% uncertainty target of the project. The main measurement errors are measurements of the top electrode areas (measurement repeatability, pitch AFM calibration, and tip profile determination) and the measurements of the SiO2 layer

thickness (repeatability and height AFM calibration). The impact of humidity (from 1% to 37 %) has been studied with the conclusion of a small influence in certain cases or no noticeable variation in other cases. The uncertainty values thus depend on the performances of the AFM used to measure the dimensional parameters of the capacitor and on the instruments used to dimensionally calibrate this AFM.

Traceability of impedance measurements with SMM instruments has been established by METAS and LNE through the realisation and characterisation of capacitance, inductance and resistance standards.
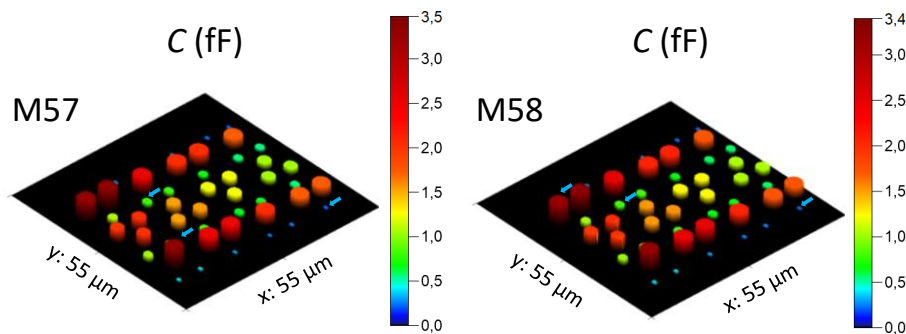
Figure 3: Calibrated capacitances on two samples.

LNE and METAS have strongly collaborated on the measurements of piezoelectric samples provided by SURREY). In order to deposit gold pads on top of the surface a specific design of pads was carried out by LNE. In **Figure 4**, a schematic cross-section view of the produced PZT sample and the AFM topography image produced by METAS are provided. Permittivity of PZT piezoelectric samples have been obtained by METAS ($\varepsilon_{PZT} = 121$) and by LNE ($\varepsilon_{PZT} = 373$).
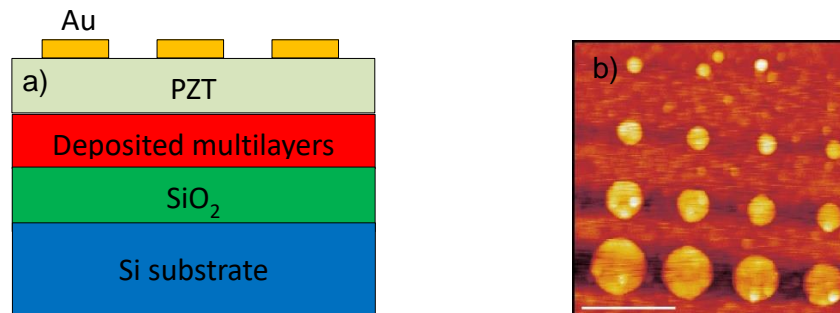

Figure 4: a- A schematic cross-section view of the produced PZT sample. b- AFM topography image obtained with SMM instrument of METAS.

Metrology platform – part 2: stress and strain measurements as well as structural analysis based on analytical in-situ X-ray (XRD, GIXRF-EXAFS techniques

The development of ultra-low power energy-efficient devices needs the correlating of material structures and device functionality with different material properties. Advanced materials such as piezoelectric materials must be characterised with the use of in-operando and in-situ techniques under different conditions: temperature, pressure, stress, strain, electric and magnetic fields. Small physical displacements of the sample surface can be measured using an interferometer, with X-ray diffraction showing structural information and atomic strain. In ADVENT, the complementary techniques of X-ray diffraction were adapted to such new classes of materials (piezoelectric) and have been considerably improved by project partners PTB, ULiv and SURREY in terms of capabilities, traceability and reliability. BAM has produced lamellae adapted to this variety of techniques.

X-ray diffraction (XRD) allows the characterisation of crystalline and polycrystalline materials in a non-destructive manner and can provide information on phases, preferred crystal orientations (texture), and other structural parameters, such as average grain size, crystallinity, strain, and crystal defects. In extended X-ray Absorption fine structure (EXAFS) measurements the short-range order is probed while X-ray diffraction probes the long-range order of a sample. In other words, the nearest-neighbour configuration is subject to the measurement in EXAFS, while X-ray diffraction measures the distance between the crystalline planes

contributing to the diffraction peak. In contrast to XRD, EXAFS provides element-specific information since this technique is based on the photoelectric effect. Thus, both techniques provide complementary information.

Surrey supplied pure crystal and ceramic samples of 1 μm thick film for X-ray measurement technique evaluation. The chemical composition of pure crystal and ceramic samples are respectively SIO2/Ti/Pt/LNO/PZT and TiN/STO/LNO/PMN-PT.

The thin film samples (**Figure 5**) were delivered with and without Au electrodes on the top for structural investigations and in-situ studies with electromagnetic fields or stress/strain evaluations. In the case of samples with top electrodes, small circular gold electrodes were evaporated on the top surface onto which an electric field was applied. Independently of the technique used, great care was taken to ensure that the incident x-ray beam was in fact hitting the appropriate electrode that was applying potential to the PZT film

To explore piezoelectric and piezoresistive devices, PTB, ULiv and SURREY have considerably increased the capabilities of XRD and EXAFS techniques and improved the measurement capabilities in Europe.
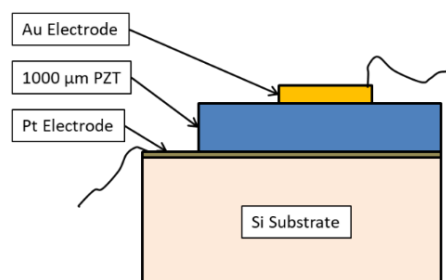

Figure 5: Scheme of the sample layout (PZT sample shown here) with the Au electrode deposited on the top.

ULiv and SURREY worked on the development of an in-situ stress cell and on the improvement of in-situ X-Ray PE loop system on the XMaS beamline at European Synchrotron Radiation Facilities (Grenoble, France).Before the ADVENT project , the sampling frequency limitation of the X-Ray PE loop system was 40 KHz ADC and it was possible to explore sensitivity to field and to frequency up to 1 MHz conditions. As a result of the ADVENT project it is now possible for the loop to reach 100 kHz makingmeasurements up to 20 MHz possible. This increase in frequency has been possible mainly through modifications of the current amplifier and analogue to digital conversion part in the experimental setup. The in-situ stress cell was designed by project partners SURREY, ULiv and Alistair Harris of Design-Mecanique (France). The cell is based on a piezo servo controller and a piezo server actuator, which are integrated into a rigid assembly (**Figure 6**). Responses of single crystals to electric fields (up to 0.1 MV/cm), magnetic fields (up to 3T), stress/strain (up to 60 MP and over 103 μstrain) and temperature (up to 450 K) were investigated by PTB using EXAFS electric field only and ULiv and SURREY using XRD ().

At PTB, a novel experimental scheme was developed and tested in which time resolution is not restricted by the read-out speed of the detector but dictated by the repetition rate of the excitation source available, in this case a synchrotron radiation source. In this novel concept, the AC electric field to be applied needs to be synchronized with respect to the arrival time of the incident X-ray pulses in order to ensure that each time an X-ray pulse is incident on the sample the same electric field is applied. This concept then allows integration over many X-ray pulses in order to ensure that sufficient counting statistics for the X-ray fluorescence signal can be achieved. The concept of the time-resolved (dynamic) experiments to be realised at a frequency above 2 MHz was thoroughly applied to AC electric fields.
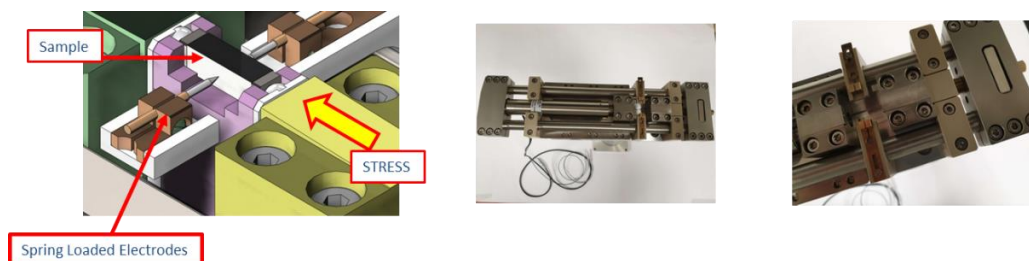

Figure 6: Illustration of the experimental configuration when using the stress cell and pictures of the stress cell after assembly.

A summary of main results obtained with the new stress, strain and in-situ X-ray measurements capabilities developed in ADVENT is presented below:

- The XRD studies with time-dependent electric fields were able to detect changes in the lattice spacing while no changes in unit cell distortions were identified by means of EXAFS.

- Either EXAFS is significantly less sensitive than XRD for this type of measurement or the sample show different response in the short-range order explored by EXAFS and the long-range order explored by XRD.

- Responses of single crystals to electric fields (up to 0.1 MV/cm), magnetic fields (up to 3T), stress/strain (up to 60 MP and over 103 µstrain) and temperature (up to 450 K) were investigated as well by EXAFS (electric field only) and XRD.

- Stress, strain, X-Ray intensity, and field are all measured simultaneously and recorded using a new developed data acquisition system.

- X-ray intensities and analogue voltages up to 24 bit resolution has been recorded with a sampling rate of 40 kHz and for a range of sample diffracting planes as a function of mechanical strain (**Figure 6a**).

- Ferroelectric hysteresis loops were measured with an applied magnetic field, (**Figure 6b**). There is a statistically significant change in the ferroelectric response with applied magnetic field, notably in the material's electric coercive field EC. To the best of our knowledge, there are no reports showing the coexistence of these phenomena and the only previous reports on multiferroicity do not measure or they explicitly state that there is zero magnetoelectric coupling.

- Grazing-incidence X-ray diffraction on a single PIN-PMN-PT crystal was used to study in-situ the dependence on the electric field and demonstrate the non-uniformity of the effective piezoelectric coefficient near the surface. Temperature and depth effects on the field-dependent strain were measured for several different lattice planes. A measurable depth dependence of lattice parameter and calculation of in operando strain identifies those planes that have a higher sensitivity to field.
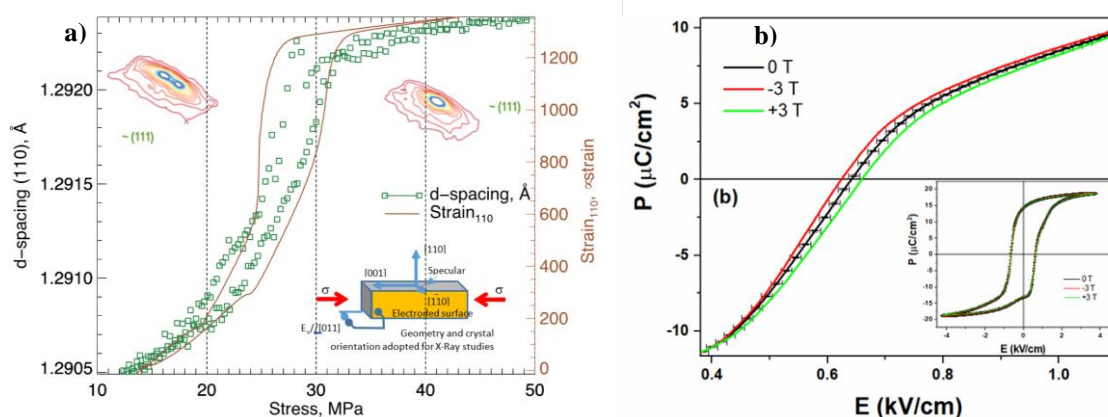

Figure 6: a) In-situ X-ray diffraction of the (110) reflection (d-spacing - green squares) compared to macroscopic strain (solid line) measured as a function of applied uniaxial stress at zero applied field. b) Polarization vs. electric field curves at 0 T and (±)3 T applied magnetic fields measured on a $BaTiO_3$ single crystal mounted within a 4 T superconducting magnet.

Metrology platform – part 3: in-situ electric field and strain based on TEM and IRSNOM techniques

Transmission Electron Microscopy (TEM) holographic methods and Infrared Scanning Near-Field Optical Microscopy (IR-SNOM) were investigated and optimised in ADVENT to measure in-situ strain of piezoelectric and ferroelectric materials. Focused Ion Beam Milling (FIB) sample preparation was required to support such advanced techniques. These techniques provide alternative characterisation methods to resolve mesoscale structures including ferroelectric domains, complementary to the diffraction methods previously described in previous section (Metrology platform – part 2).

1. TEM technique – method and results

TEM remains a highly invasive technique, where a thin lamella must be extracted from the bulk sample for analysis. TEM techniques can be used in conventional electron holography techniques and in more recent

dark-field electron holography approaches. Both are based on the interference of two waves propagating through two different media resulting in phase differences that can be recovered directly from the hologram by image processing techniques. The phase is important because it contains information about the electric and magnetic fields in and around the sample. In dark-field electron holography setups, one medium is a strain-free region of crystal. The resulting phase difference is then related to the strain in the sample.

In both conventional and dark-field electron holography, a field-free reference wave is required. This poses a problem for biasing experiments where large electric fields can create long-range perturbations to the electron wave, as this is the case for the study of piezoelectric materials. In consequence, the sample geometry (**Figure 7**) and holder **(Figure 8)** have been extensively investigated by BAM and CNRS respectively.

BAM has developed the protocol for preparing and contacting the TEM lamella to the support grid that is composed of 5 main steps (**Figure 7**):

The sample preparation for in-situ TEM remains a tour de force, particularly when a thin-layer needs to be contacted for the bottom electrode. The full procedure can take 8 hours of FIB and there is no guarantee of success. Having said that, the success rate has increased over time and is now well over 50%. The major improvement in sample preparation is the result of strong collaboration between CNRS and BAM.
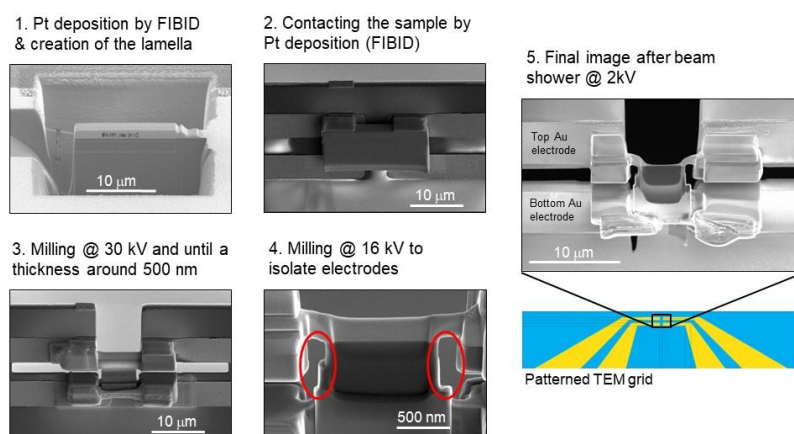

Figure 7: Procedure developed by BAM for TEM lamella preparation and contacting by FIB: lift-out, milling, contacting to electrodes.

Figure 8: New approach developed by CNRS to in-situ biasing experiments: from chip-based TEM holders to patterned TEM grids and FIB thinned and contacted samples.

Regarding in-situ TEM experiments, CNRS carried-out measurements on nanocapacitors and PZT samples. The in-situ biasing capabilities were tested on nanocapacitors made of a dielectric (**Figure 9**). The conducting substrate was used as the bottom electrode facilitating the specimen's preparation. Conventional electron holography was carried out on the samples whilst different (DC) biases were applied successively to the electrodes.

The first main result of the TEM method is the change in phase that can be seen across the dielectric from the top (blue) to the bottom (red) electrode (**Figure 9**). Within the electrodes, the phase is uniform but in the vacuum region and across the dielectric, the phase varies continuously. The phase shift is in fact linear with the integrated electrostatic potential along the path of the fast electron, with the constant of proportionality depending only on universal constants and the accelerating voltage.
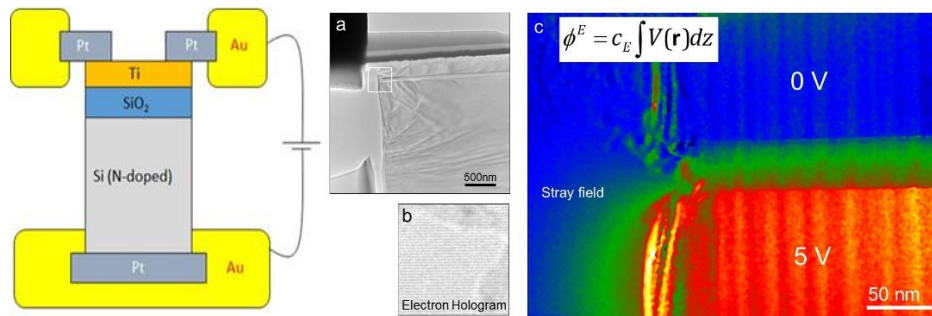
Figure 9: Right: test structure specimen of a MOS (Metal-Oxide-Semiconductor) nanocapacitor. Left: In-situ electron holography of a nanocapacitor: (a) bright-field TEM image of the connected sample, with box showing region of interest; (b) detail of the electron hologram; (c) map showing electrostatic phase for 5V applied bias. Phase shown in false colours.

The second main result of the TEM method was its application to PZT samples under in-situ TEM conditions. Some experiments were required to make sample contacts compatible with TEM measurement set-up. The sample successfully sustained a bias of up to 5 V which is equivalent to 450 kVcm-1 across the thin PZT layer. Domain wall motion could be triggered with high reproducibility. As a demonstration of the new possibilities of studying local electric fields in piezoelectric materials, the difference in phase between two configurations of polarisation was determined (**Figure 10**). The electric field is not the same in one domain due to the change in polarisation. Extensive modelling will be required to understand fully these first encouraging results.
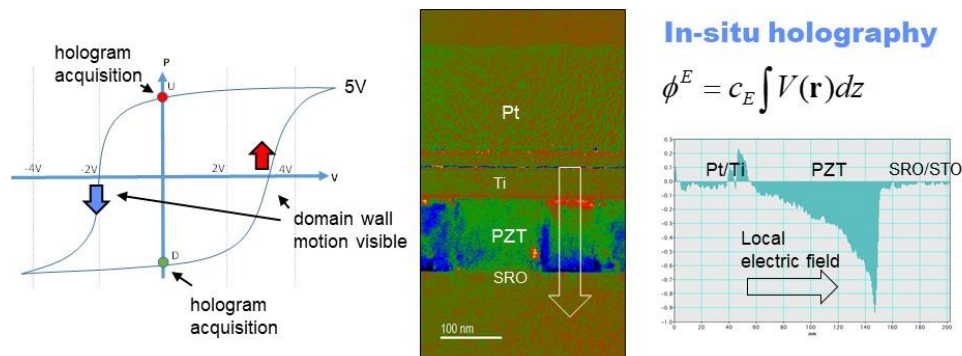

Figure 10: In-situ electron holography of PZT sample: sketch of the experimental hysteresis loop indicating domain wall motion and polarisation flip; hologram phase difference between two polarisation states (red and green on hysteresis loop); profile of phase variation showing steep gradient within one domain indicating the presence of a local electric field.

2. Near-Field Optical Microscopy (IR-SNOM) – method and results

For conventional optical methods, the diffraction limit only allows spatial resolution of the order of the wavelength preventing nanoscale spatial resolution. This is the reason why the optical method of IR s-SNOM (Infrared Scanning Near-field Optical Microscopy) was also be investigated by PTB in ADVENT since the diffraction limit is no longer relevant. The technique is based on focusing light on a metallic material, resulting in strong electromagnetic near fields at the tip apex that polarize the sample within a confined volume and re-radiate scattered fields. Secondly, mechanical signals from the tapping cantilever at the same location where the optical signals originate are provided simultaneously. The measurements in ADVENT were done using a commercial IR-SNOM. The Nano FTIR configuration (illumination with spectrally broad radiation) with synchrotron illumination from the Metrology Light Source (MLS) was used at PTB Berlin.

As for TEM experiments, a very careful preparation was developed by BAM to optimise the sample for in-situ IR-SNOM requirements. To prevent unwanted contaminations the modified lamella is attached to the platform, and thin-deposited Pt strips provide conductive connection. This innovative technique prevents Pt contamination that induce leakage currents and permits strain measurements by the IR-SNOM technique.

In-situ IR-SNOM measurement was performed on a PZT sample after having been prepared using the FIB milling technique optimized by BAM (**Figure 11**). Using a piezoelectric constant of PZT in around d33 = 400 - 800 pm/V and a thickness of the PZT layer of 580 nm we conclude that a strain of ε = 0.7 - 1.3 % can just be

resolved in the current setup. With the tip-diameter being the main factor determining the spatial resolution strain inhomogeneity can in principle be resolved to approximately 10 nm.
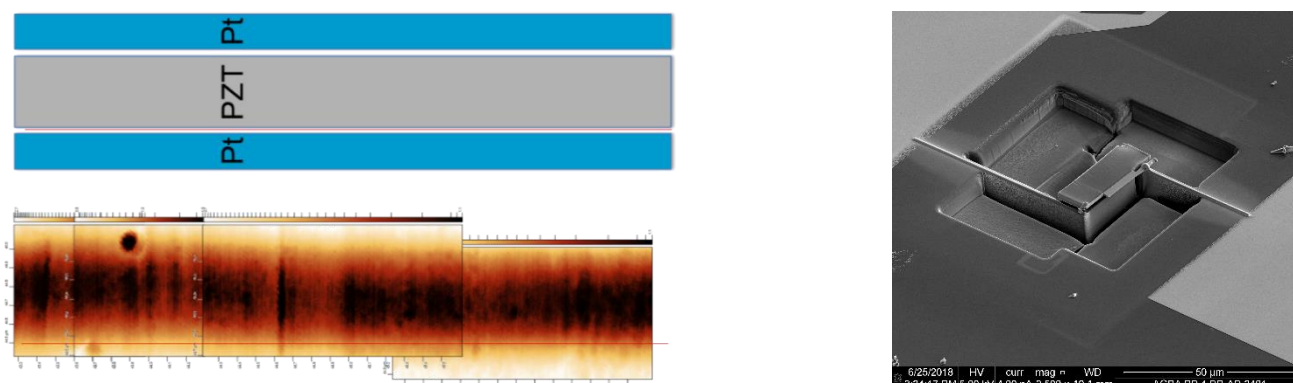

Figure 11: Left: Imaging of the PZT region sandwiched between the two Pt contacts, shown schematically above, and matching with the measurements below. Right: Modified PZT-lamella on pre-milled platform between gold pads and chip using this (innovative) technique developed by BAM.

Objective 1 - Conclusion

Impedance standards (capacitance, inductance and resistance) for Scanning Microwave Microscopy (SMM) were established and the precision of this technique under different environmental conditions with respect to the humidity level were investigated. Sample preparation and characterisation techniques for ferroelectric and piezoresistive materials were advanced. For X-ray based works experimental schemes for time-dependent measurements were developed towards the MHz regime and a versatile calibrated stress rig for characterising single crystal materials has been realised. Thin film piezoelectric samples were investigated when applying electric fields (0.1 MV/cm) and single crystals when applying, magnetic fields (up to 3T), stress and strain (up to 60 MP and over 103 µstrain) or temperature changes (up to 450 K). A breakdown of thin film samples was observed when higher levels for electric fields and stress than those mentioned previously were applied during experiments. That explains the difference to the 4MV/cm, strain 0.02% and stress of 200MPa given in the deliverable title. In other words, all required in situ operando metrological tools needed to achieve levels defined at the beginning of the project have been developed during ADVENT but have not been applied to the higher levels initially anticipated due to sample limitations. The metrological capacity of transmission electron microscopy (TEM) was established during in-situ biasing experiments on piezoelectric materials. Imaging by means of IRs-SNOM allows strain mapping across surfaces of IR active materials. This objective has been fully achieved.

Objective 2: To develop frequency and time-domain techniques for the simultaneous measurement of dynamic thermal profiles, electro-magnetic field sensing, DC electrical power consumption and RF operating waveforms for a wide range of RF electronic components (operating in-situ, under realistic conditions). These techniques to be combined with a multi-physics approach, which will establish rigorous energy budgets, and diagnostic capabilities, for a wide range of electronic components (operating in-situ, under realistic conditions), required for next-generation communications. The uncertainty in the measurement of the power efficiency to be reduced to less than 1 %.

The characterisation of RF and microwave components can be achieved by using contacting (time domain technique using oscilloscopes, frequency domain using VNAs) and non-contacting (thermal mapping, electromagnetic field sensing) methods. Before the start of ADVENT, no metrology basis existed in Europe for measuring simultaneously and in-operando the electromagnetic and thermal responses of RF and microwave components under realistic operating conditions, nor for accurately measuring switching losses and material properties of real components at nanoscale with established traceability to SI.

This objective of the project has contributed to improve frequency and time domain, electromagnetic field, material properties and thermal mapping measurement techniques and has provided traceability and reliability of data produced by these techniques. In addition to those techniques mainly developed separately during the lifetime of the project, a multi-disciplinary approach has been investigated to characterise microwave transistors in terms of energy budget and distributed performances. This multi-physics approach represents a

promising opportunity to reduce measurement uncertainty for determining power efficiency in existing and the next generation of electronic components.

In this part of the report, firstly, we describe the main measurement results obtained with thermal distribution and temperature, material properties and various electromagnetic techniques as well as associated uncertainties; secondly, we describe the method and results of the multi-physics approach.

Contacting and non-contacting techniques to measure thermal distribution and temperature of electronic components

Due to the scaling reduction and increase of density of components in circuits, thermal issues represent one of the main challenges for industry developing integrated components and electronic devices. In this part, we will describe briefly new measurement capabilities and uncertainties for the following:

- Scanning thermal microscopy (SThM) and Infrared imaging optics (infrared microscopy)
- Thermoreflectance-based thermal mapping (TM)

1. Scanning thermal microscopy (SThM) and Infrared imaging optics (infrared microscopy)

Two methods have been used by CMI to map the surface temperature on active electronic devices. Scanning Thermal Microscopy (SThM) represents a contact method with nanometre resolution and is based on the use of a tiny resistive temperature sensor that is scanning the surface. Infrared microscopy represents a non-contact method with resolution limited by the infrared radiation wavelength. The two methods are complementary and can be combined using a hybrid data measurement approach. For all the measurements, a custom-built SthM/IR head has been used that can combine both methods. Using both techniques, different samples have measured in various phases of the ADVENT project. For the purposes of this report, we have chosen two representative samples. First, the Cree HEMT (High electron mobility transistor) CGH40010F and second, the bipolar transistor 2n3439.

Scanning thermal microscopy (SThM) is a technique based on a wire probe that scans over the surface of a sample. The wire changes its electrical resistance and represents a resistance thermometer detector (RTD). The temperature calibration curve must be determined independently in order to calculate the temperature of the sample. Each and every SThM tip should be calibrated as the variability between the individual probes is high even within the same production batch. The spatial resolution of SThM is usually much higher than that of infrared methods, as it is not limited by the wavelength used.

Before measuring the bipolar and HEMT transistors (**Figure 12**), the microscope probe was calibrated in a temperature regulated thermal oven while connected to the SThM circuitry in the same way as during normal scanning. All the settings of the apparatus were left unchanged between the calibration and the measurement. **Figure 12** is a temperature profile of an HEMT transistor in operation.
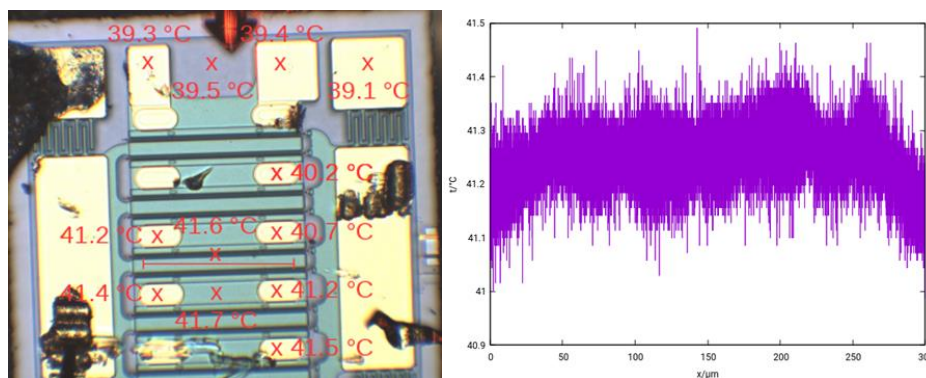

Figure 12: (left) optical image of the HEMT transistor (SThM probe shown on the top side), with individual temperatures and a profile marked on it, (right) the temperature profile.

Infrared microscopy used for measuring temperature is based on detection of thermal radiation, which is a widely used method in various fields. It has many advantages as it is relatively simple to use, non-contact and fast. On the other hand, some drawbacks limit its potential and impose complications. Its resolution is limited by the wavelength detected, which is around 10 micrometres. This is a significant limitation for the measurement of microelectronic chips, but the method was tested anyway. Moreover, carefully designed optics must be used in order to make a high-resolution infrared microscope.

Another challenge arises from the fact that the radiated intensity depends on the emissivity of the surface. Without knowing the emissivity, the temperature cannot be calculated. The emissivity depends on the material of the sample and on morphological properties, e.g. roughness.

The accuracy and precision of temperatures measured cannot be easily specified as it depends very much on the emissivity of the surface and the time spent on the measurement. Several different situations were analysed with a worst-case result of T = (112 ± 23) °C and a best-case result of T = (167.50 ± 0.14) °C. The main uncertainty contributions are apparatus noise, statistical model flaws (required to get fitting errors on specific parameters), and temperature measurement.

2. Thermoreflectance-based thermal mapping (TM)

The transient Thermoreflectance microscopy system is based on the Thermoreflectance principle where the relative change in reflectivity from the surface of the Device Under Test (DUT) with respect to temperature change is captured by the CCD camera. The Cree GaN transistor was measured by SURREY in steady state and transient modes with a DC bias only and with DC bias and microwave stimuli. Results demonstrate the ability of Thermoreflectance to measure temperatures across a real device under operational conditions (**Figure 13**).
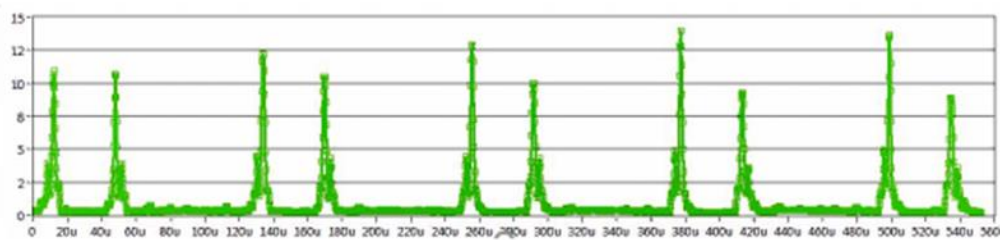

Figure 13: Transient temperature results of the top 10 fingers of the transistor obtained at maximum efficiency showing a non-uniform finger-to-finger heating for the first 200 us of the operation of the device.

Scanning Microwave Microscopy to provide material properties of real devices

METAS and LNE have used an in-house-built SMM and a commercial SMM respectively to perform material and electrical property measurements on real devices. From reflection coefficient S_{11} of the sample measured by SMM (VNA associated to AFM), it is possible to extract impedance and material properties. The device selected provided by ULILLE was a GaN transistor. LNE and METAS have measured the same samples and obtained similar observations. The amplitude and phase maps show a contrast difference between above 2 μm thick Au, Pt regions (Pt dep. and Pt/Au-rich layer) and GaN layers, which indicates the different electrical properties for those materials. However, the difference in $\Delta S_{11}m$ (in both phase and magnitude maps) between SiC substrate and AlGaN layer is unnoticeable. Despite a special sample polishing developed by BAM, it was possible to observe borders of different materials from images but not to determine their material properties values.

Time domain technique to measure RF switching losses

The methodology developed in ADVENT focuses on the characterisation of the losses in high-speed switching devices for power electronics applications with rise time in the nanosecond range, thus having significant spectral components up to, approximately, 1 GHz. This is the case of GaN FET power transistors employed in hard-switching power converters. For this purpose, the time-domain techniques were employed by UPC for measuring the instantaneous power losses, $p(t)$, in GaN FET (either of depletion mode or of enhancement mode). In that sense, the drain-source voltage, $v_{DS}(t)$, and the drain current, $i_D(t)$, are measured using contacting probes and real-time sampling oscilloscopes.

Time-dependent behaviour of the power loss in the switching device can be summarised in three main regions with corresponding energy losses (**Figure 14**): the turn-on and turn-off transitions regions, and the conduction region. Switching (energy) losses (E_{on} and E_{off}) occur in the turn-on and turn-off regions and energy dissipated during the conduction state, E_{cond}. High speed switching devices losses can be summarised as follows: dynamic losses (turn on and turn off losses, gate charge losses, reverse conduction losses, dynamic COSS-related reverse conduction losses, and reverse recovery losses), and static losses (conduction loss, inductor loss, and other losses).
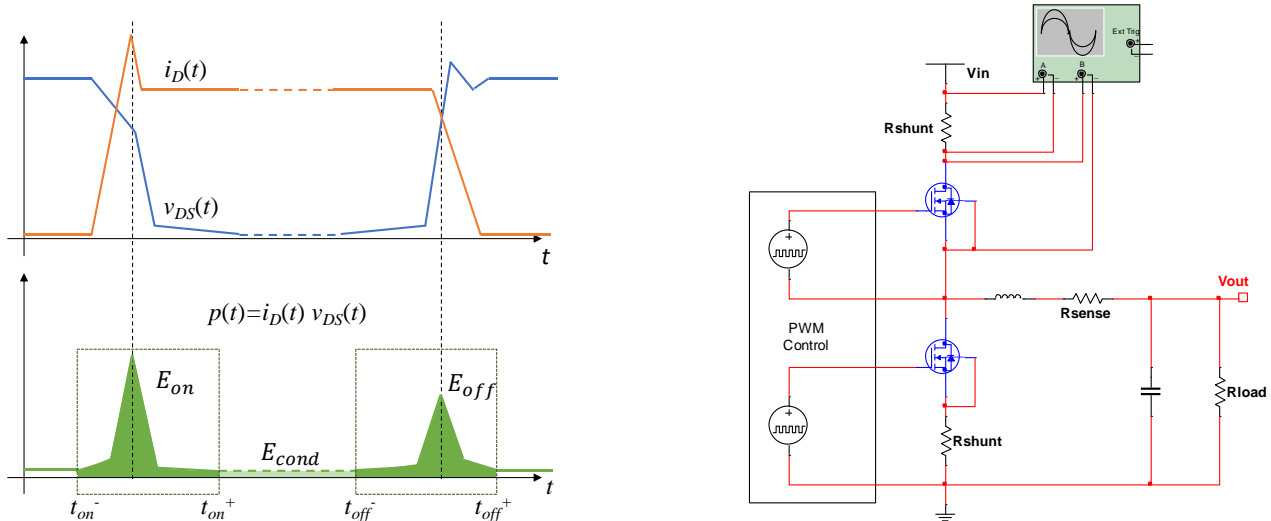

Figure 14: Instantaneous power loss in switching devices (right) and set-up used for time domain technique.

The total switching losses, P_{SW}, is defined as,

$$P_{SW} = f_{sw}(E_{on} + E_{off}) = f_{sw}\left[\int_{t_{on}^-}^{t_{on}^+} p(t)dt + \int_{t_{off}^-}^{t_{off}^+} p(t)dt\right]$$

Where f_{SW} is the switching frequency, and [t_{on}^-, t_{on}^+] and [t_{off}^-, t_{off}^+] time intervals of the turn-on and turn-off transitions, respectively

Measuring the current waveform is challenging because oscilloscope current probes (hall effect and Rogowski probes) have shortcomings for this application. In this regard, current probes are too large for fitting in the power converter, and even if it were possible to do so, the insertion impedance of the current probe would be significant compared to the circuit, thus affecting measurement accuracy. Therefore, in practice, current probes are not suitable for this purpose. With oscilloscope current probes discarded, sensing resistors such as coaxial shunts and planar resistors are a reasonable alternative for transforming the current waveform into a voltage waveform to be measured.

An appropriate test bench is necessary, but not sufficient, for ensuring accurate measurement of the switching losses. This is because the probe-oscilloscope system introduces distortion in the waveform, particularly when the probe's input capacitance is of the same order of magnitude as the capacitance of the DUT. To overcome issues related to the distortion of the probe-oscilloscope system UPC has developed circuit modelling and performed simulations.

For characterising the losses in GaN FET transistors in a switching regime, it is necessary to operate the device through a circuit that is representatives of its intended application and exercising it within its specified ranges. For instance, loss components are a function of the switching frequency and drain current. In this way, it is possible to obtain performance figures that are meaningful in terms of electronic design for highly power efficient applications. This is the reason why UPC has decided to perform the measurements over real evaluations boards**.** The power losses were analysed at three different switching frequencies, 100 kHz, 1 MHz and 5 MHz, corresponding to the minimum, optimum and maximum values for the specified switching frequency. It is important to note that final measurements were performed inside an anechoic chamber to avoid coupling RF noise into the waveforms. This consideration is important to improve the signal to noise ratio in the measurements. The RF noise coupled into the measurements cannot be filtered because the waveforms have a bandwidth in the order of hundreds of megahertz. **Figure 15** illustrates the measurement results obtained at 5 MHz.
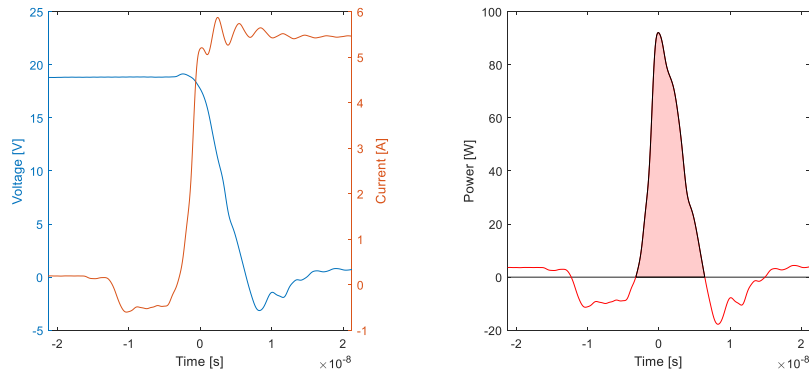
Figure 15: Switching loss for the turn-on transition for f_{sw} = 5 MHz and I_L = 5 A.

UCP has provided an accurate and traceable evaluation of switching loss measurements that created the opportunity to realise an analysis of the loss components. This later consists of an analysis of the distribution of the different contributions to the total losses that emerge from distinctive phenomena that occur during the switching process. It allows the generation of an understanding of which aspects should be controlled, from an electronic design point of view, for optimizing the efficiency of the circuit.

In addition to the measurement results, UPC has also provided a very detailed uncertainty budget of power switching losses P_{SW}. The uncertainty in the measurement of P_{SW}, u (P_{SW}) can be calculated as:

$$u_{P_{SW}} = \sqrt{(f_{SW}u_{SW})^2 + \left(E_{SW}u_{f_{SW}}\right)^2}$$

Where $u_{f_{SW}}$ is the uncertainty in the measured switching frequency f_{SW}, u_{SW} is the combination of the measurement uncertainties of the switching losses during the turn-on and turn-off transitions and E_{SW} is the energy of the switching losses. Considering $E_{SW}u_{f_{SW}} \ll f_{SW}u_{SW}$, then the approximation $u_{P_{SW}} \approx f_{SW}u_{SW}$ is sufficiently valid. This means that the measurement uncertainty in the switching power losses are proportional to the switching frequency. **Table 1** below gives uncertainty values of the power switching losses. In the test conditions exercised, the uncertainty in the measurement of the switching loss was approximately between ±1% and ±8%. It is not possible to provide an overall general estimate of the measurement uncertainty resulting from applying this switching loss measurement method, that is, the measurement uncertainty must be calculated for the particular test conditions and test setup.

Table 1: Energy Losses and associated uncertainties.

f_{SW}	I_L	E_{SW}	P_{SW}	$u_{P_{SW}}$		$U_{P_{SW}}$ for k = 2	
(MHz)	(A)	(µJ)	(mW)	(mW)	(%)	(mW)	(%)
0.1	1	0.1487	14,87	±0,36	±2,42	±0,72	±4,84
1	1	0.1016	101,6	±3,11	±3,06	±6,22	±6,12
5	1	0.8500	4250	±19,91	±0,47	±39,82	±0,94
0.1	5	0.3452	34,52	±1,41	±4,08	±2,82	±8,17
5	5	0.4433	2216,5	±74,48	±3,36	±148,96	±6,72

The uncertainty in the measurement of the power conversion efficiency has also been evaluated by UPC in the framework of ADVENT. In this case, power efficiency is defined as below where

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}I_{out}}{V_{in}I_{in}} = \frac{V_{out}I_{out}}{V_{out}I_{out} + P_{total}}, \tag{16}$$

Where V_{out}, I_{out}, V_{in} and I_{in} are the DC output and input voltage, respectively, and P_{total} is the total power loss as defined in the power budget in deliverable report D5.

For output currents that drive the power converter circuit to the optimal operating conditions, the relative uncertainty approaches the ±1% target.

Electromagnetic quantities: field sensing and RF operating waveforms measurements

Test engineers use VNAs to evaluate the performance of devices under realistic operating conditions, rather than classical single-tone test conditions that do not expose the true operating characteristics of the device. In addition, the impedance that the device 'sees' at its inputs and outputs can be adjusted using source- and load-pulling techniques to further replicate the true operating conditions of devices when they are embedded into an overall electronic circuit.

1. Source-pull and load-pull (SP & LP)

Load-pull and source-pull measurements of the Cree GaN transistor were performed by NPL and SURREY in the time- and frequency-domains using a nonlinear vector network analyser (NVNA). Mechanical impedance tuners were used to control the source and load impedances seen by the device at the fundamental frequency (3.5 GHz). The transistor characterized by NPL and SURREY has low input and output impedances of the order of 5 Ω. Therefore, a load-pull test fixture was built incorporating a 10:1 impedance transformer.

The measured output power, efficiency and power dissipation are plotted against the input power (**Figure 16)**. There is a trade-off between the maximum output power and the maximum efficiency obtainable from the device. In addition, higher output power results in a higher power dissipation, which means that increased heating will occur within the transistor.
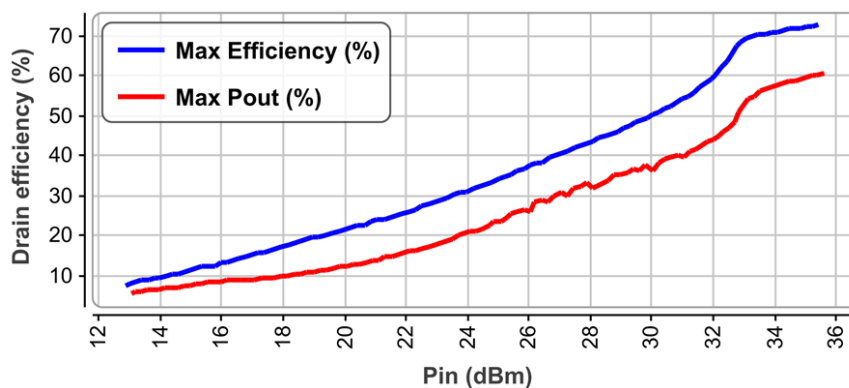

Figure 16: Measured output power and efficiency of the GaN transistor.

2. Electro-optic-based electromagnetic field sensing (EFS)

NeoScan electro-optic-based electromagnetic-field sensing (EFS) system (electric field measurement system) were set up by SURREY and training on their operation was provided to NPL users. The electric field above the device was characterised under "max Pout" and "max efficiency" conditions by setting the load tuner to the two impedance values. The normal component of electric field was measured. In this work the electric field values are presented normalised to the maximum field value observed in the "max Pout" condition. As shown in **Figure 17**, the "max Pout" field distribution is slightly wider than the "max efficiency" distribution and has a slightly higher amplitude. The electric field distributions obtained cannot be attributed solely to the channel areas of the device, but also have contributions from the source, gate, drain and bond wires of the transistor.
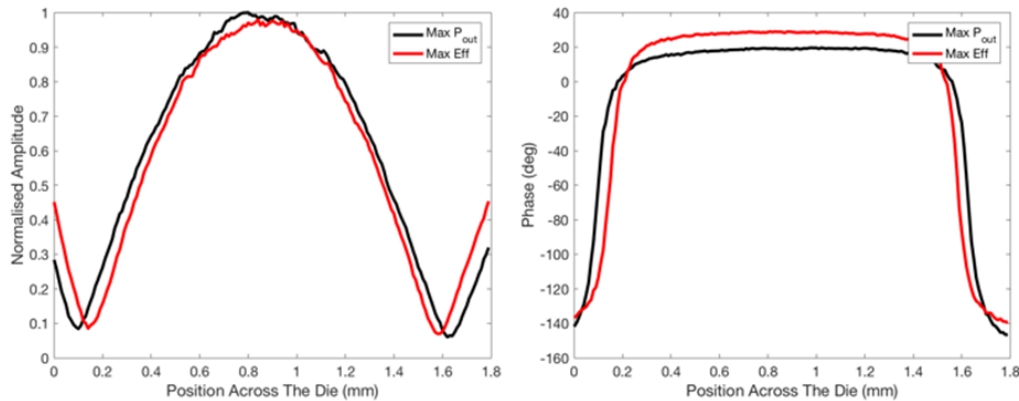
Figure 17: Measured normal electric-field component above the transistor area, at (red) maximum efficiency and (black) max output power.

Multi-physics approach to measure the performance of high frequency electronic components operating under realistic conditions

A multi-physics approach has been applied by NPL and SURREY to provide performance metrics for four HEMT transistors (CGH40025) selected as device under test (DUT). In the multi-physics approach applied in ADVENT, Load-Pull and Electro-optic Electric Field Sensing techniques have been combined as well as Load-Pull and Thermoreflectance Temperature techniques to the same set of four devices (HEMT transistor) (**Figure 18**).
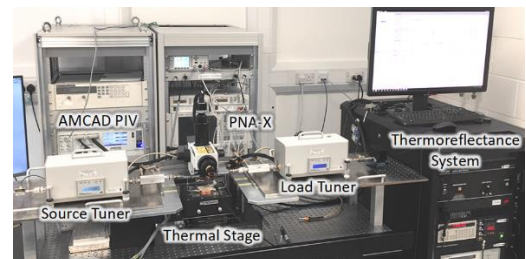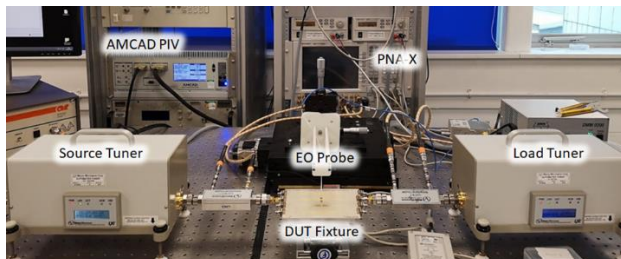

Figure 18: Load-Pull and Electro-optic Electric Field Sensing techniques combined (left) and Thermoreflectance Temperature techniques combined.

All four DUTs were measured with the load impedance (Z_{load}) set to that corresponding to maximum power added efficiency PAE and to that corresponding to maximum Pout as determined during the load-pull measurements. At the two load conditions, measurements were made of Pout, PAE, DC power (Pdc) and dissipated power (Pdiss) for different values of the input power (Pin). **Figure 19** shows only the PAE measurement results for one of the DUTs.

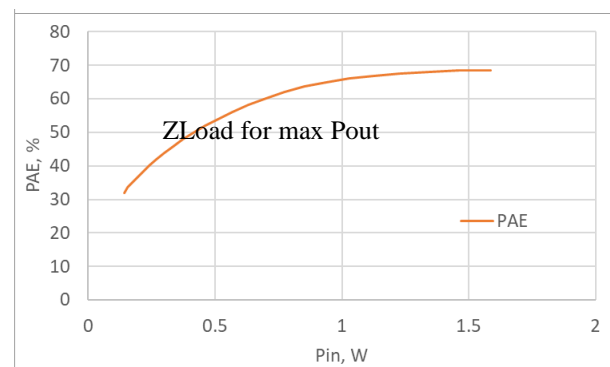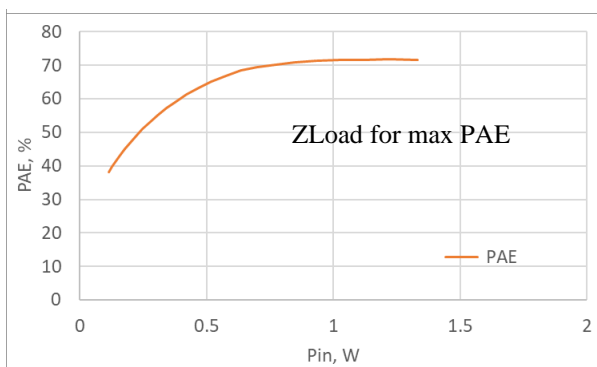**Figure 19**: Measurements of PAE obtained for one of the DUT under specific impedance load condition.

Objective 2 - Conclusion

SMM and AFM have been applied to characterise real devices at the wafer level. The use of the Thermoreflectance system has been extended to investigate the extent to which pulsed measurements of on-wafer transistors are isothermal. The infrared method for the measurement of temperature has been improved and measurements on real devices have been obtained with an uncertainty of less than 0.5 °C. A time domain technique has been developed and applied to power converters and power amplifiers for measuring switching losses and power conversion efficiency. The uncertainty in the measurement of the power efficiency has been reached 1 % for output direct currents that drive the power converter circuit to the optimal operating conditions. A multi-physics approach has combined Load-Pull and Electro-optic Electric Field Sensing techniques as well as Load-Pull and Thermoreflectance Temperature techniques to obtain energy budgets of real devices (HEMT transistor). In this regard, maximum power added efficiency, output power and dissipated power have been evaluated under different load conditions. This objective has fully achieved.

Objective 3: To Develop embedded sensors and the associated calibration and measurement techniques to accurately measure power consumption of wireless systems (mobile phones, tablets and connected devices) and to improve the effectiveness of analogue and RF tests of components and systems. The power measurement techniques will be able to characterise and calibrate on-chip power sensors with an uncertainty of less than 10 μW.

Embedded sensors and the associated calibration and measurement techniques have been developed in ADVENT to accurately measure power consumption of wireless systems (mobile phones, tablets and connected devices) and to improve the effectiveness of analogue and RF tests of components and systems.

ULILLE has used signal-tracking techniques based on power detectors in order to improve amplifier efficiencies in 5G devices. They have established the design of two types of power detectors and the on-chip power standard required for calibration has been developed by LNE. The frequency target selected for the project was 42 GHz as this is a possible candidate for 5G deployment.

Below are presented the designs fabricated by ULILLE: a zero bias detector based on MOSFET transistor (**Figures 20**) and an adjustable power detector based on a Schottky diode both integrated in in 55-nm BiCMOS technology from ST-Microelectronics. The detectors have been characterized in terms of matching (S_{11}) and sensitivity (**Figures 21**). The power consumption is zero for the zero bias power detector and 0.07 μW and 8 μW for the adjustable power detector.
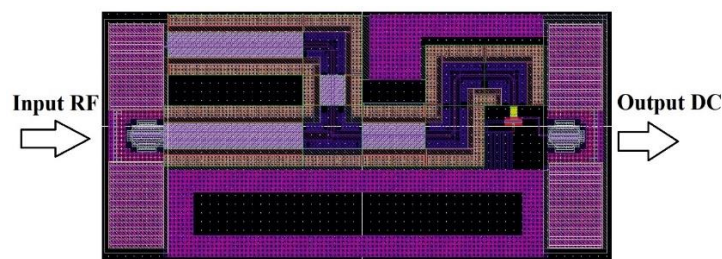

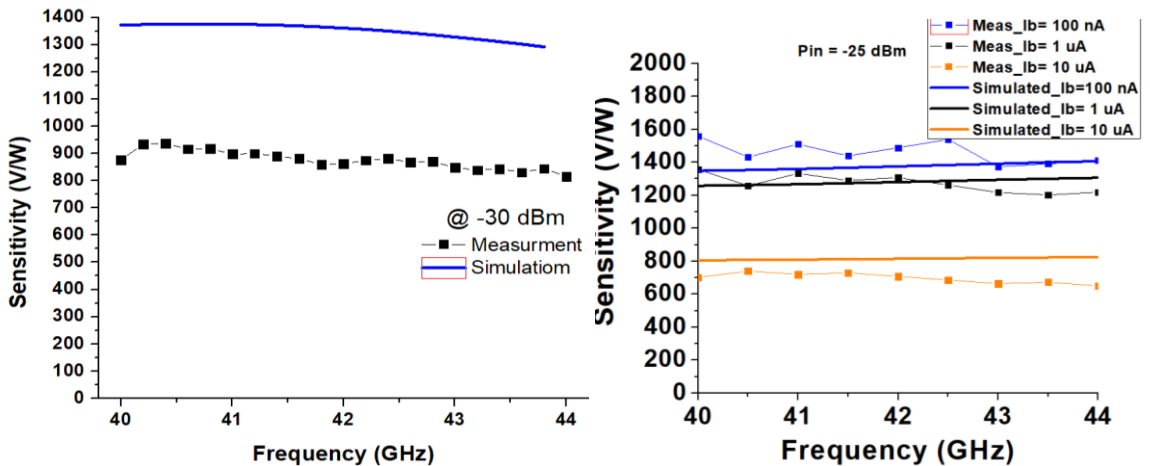**Figure 20**: Matching and sensitivity of zero bias power detector.

Figure 21: Matching and sensitivity of zero bias power detector (left) and adjustable power detector.

LNE has developed the on-chip power standard needed to establish the traceability of power measurements at the chip level. The sensor has been designed using the thermoelectric principle and simple planar structure (single layer sensor) and the layout has been produced to allow for its fabrication within ULILLE's technology plant. The sensor is composed by a 50 Ω coplanar transmission line, two 100 Ω resistors in parallel placed at the end of the CPW line and a thermopile placed at an optimised distance of the resistors (**Figure 22**). LNE characterised the power detector in terms of matching (**Figure 22**) and sensitivity.
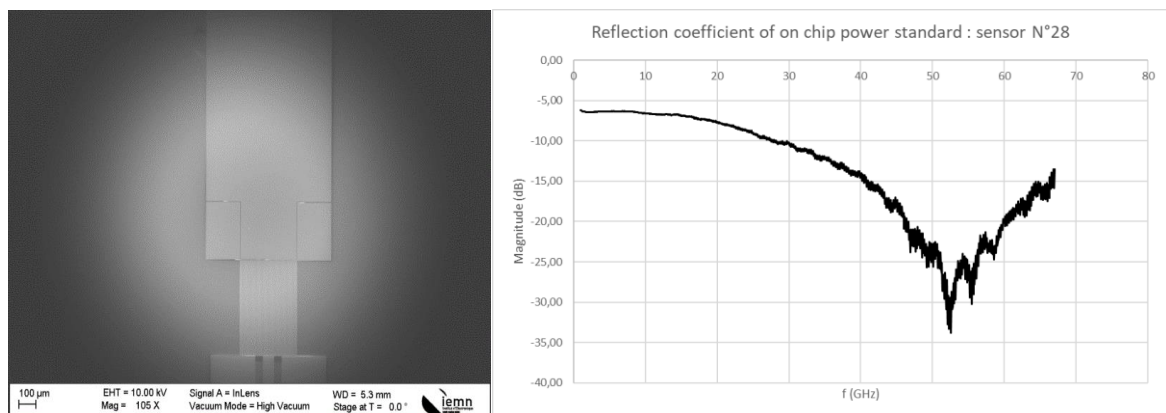

Figure 22. On chip power standard composed of a CPW transmission line, two resistors of 100 Ω each, thermopile and heat sink behind (right figure) and its input reflection coefficient (left figure).

The zero bias detector and the on-chip power standard were calibrated in their probe reference plane that corresponds to the input of these devices against a primary coaxial reference equipped with a 2.4 mm connector. The purpose of the calibration was to determine the efficiency of the 2 types of detectors: the efficiency provide to a first approximation the losses of the detectors. In table below is presented the efficiency of the on-chip power standard.

Table 2. **Efficiency measurement results – on chip power standard**

Power level (dBm)	42 GHz	44 GHz	46 GHz
14	0.293	0.272	0.269
11	0.298	0.268	0.265
8	0.294	0.264	0.260

At the millimetre to centimetre scale, the extraction of the overall power consumption and the distribution of power losses for a PCB (and more generally for any electronic devices) are normally assessed by plugging

probes at the points of interest. This power estimation includes microwave measurements on the RF lines and DC measurements on the power supply lines. This requires a large number of probes and potential configuration changes from PCB to PCB. Therefore, for production tests or prototype developments, a contactless solution is of great interest to estimate not only the power consumption of a PCB but also the locations of unexpected power losses by heat or radiation. In ADVENT, non-intrusive techniques have been developed and used within the project as an additional power measurement method for electronic devices or systems.

The first non-invasive contactless measurement method was developed by UPEM. This uses electromagnetic NF scanners sensing the field above the structure and providing an estimation of location of unexpected power losses by heat or radiation.

Figure 23: Near-field scanning systems used.

The second technique developed by JV is based on an active shunt. This latter is used to measure very small currents in a live circuit without introducing any impedance into the current path, so that the intended function and characteristics of the circuit are not changed or destroyed, but continue to work as before the shunt was introduced into the circuit (**Figure 24**).
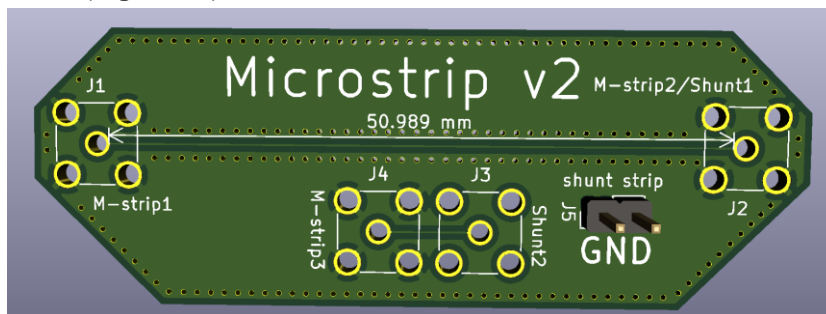

Figure 24: Example of a simple Microstrip transmission line and shunt placed both on PCB.

The traceability to both the measurement techniques developed at JV and at UPEM was provided by LNE through S parameter measurements of a reference PCB (**Figure 25**). LNE has established an uncertainty budget based on a triple evaluation: transmitted power calibration (LNE), Near-Field scanning (UPEM) and current shunt (JV).

The table below takes into account the uncertainty on both JV and UPEM methodologies based on maximum deviation against their respective reference values, and the uncertainty specific to S parameter measurements from which a reference power consumption ratio has been evaluated and provided by LNE.
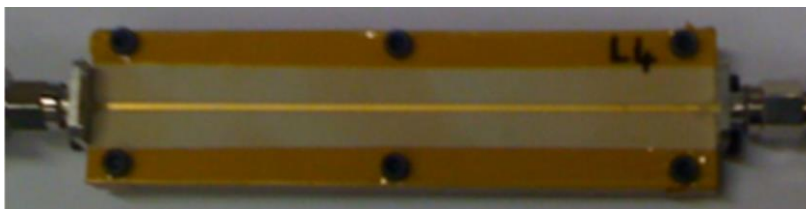
Figure 25: Reference PCB implementing a Microstrip transmission line.

Table3. **Uncertainty budget for the power consumption evaluation**

Uncertainty component	Estimate	Divisor	Standard uncertainty
NF[H] scanning (UPEM)	0.003	1.73	0.0018
Active Shunt (JV)	0.054	1.73	0.032 @ 1 MHz (0.003 @ 10 kHz)
S parameters (LNE)	0.0023	2	0.0013

Objective 3 Conclusion

Two types of power detectors, adjustable detector and zero bias detector (IEMN) have been developed in the framework of ADVENT, both suitable for low consumption embedded power measurement on 5G devices. The demonstration of a traceability route for such a measurement at the chip level also been developed within the project through the comparison with an on-chip traceable power standard. Two methods, based on different physical principles, have been developed for the assessment of power consumption on PCBs and the evaluation of their uncertainties. This leads to the comparison of a power consumption ratio estimation based on standard S parameter measurements. The presented uncertainties are associated with the power consumption ratio. Target achievement of less than10 µW will depend on the power injected in the device under test. The deliverable has been partially achieved because the uncertainty on the power ratio consumption has been estimated instead of the uncertainty of absolute power consumption. Additional absolute power measurements would had been necessary.

5   Impact

To date, 39 presentations and 6 posters have been made to conferences at various European locations, 15 papers have been accepted for publication during the lifetime of the project (these papers are all open-access publications). The project partners have submitted 3 articles to trade journals during the lifetime of this project. Two workshops and one training session took place in February 2019, September 2019 and November 2019.

A workshop "X-ray and Neutron Scattering and Spectroscopies in Ferroelectric and Multiferroic Research Workshop V" was held at IOM3 (The Institute of Materials, Minerals and Mining) in London on 4-5 February 2019. This workshop promoted project developments to 55 European, Asian and American experts from the multiferroics, magneto-electrics and ferroelectrics communities and neutron, synchrotron and spectroscopy facility end-users. Workshop participants were impressed by the high level of technical knowledge shown by the ADVENT presentations and were particularly interested in the results obtained using diffraction and Transmission Electron Microscopy methods.

A second workshop, "Microwave measurements at systems, components and materials levels: a global approach to improve energy efficiency of the next generation of electronic devices" was held in Paris during the European Microwave conference (September 2019).

The project's training course "Uncertainty in measurements for next-generation high frequency applications" was held at NPL (Teddington, UK) in November 2019 for early career stage attendees. It provided an opportunity for attendees to learn uncertainty methods, to have discussions with key high frequency metrology experts and to discover the current state of the art in S-parameters and permittivity measurements.

Impact on industrial and other user communities

A project advisory group (PAG) with members drawn from the semiconductor, electronic, instrumentation, research sectors and academia provided feedback on the projects strategy and results throughout the project via both physical and video meetings.

A meeting was organised on 9th April 2018 at LNE Trappes (France) with two key representatives from Alliance Electronique. This organisation is the major French professional union for industry and manufacturers in the electronics sector. During this meeting, a discussion was carried out to organise the dissemination of results to manufacturers and industrial members of Acsiel Alliance Electronique.

Stakeholders and collaborators of the project have already been able to take advantage of project outputs through early access to open access publications including measurement results explaining the limitations and potential functionalities of materials they are using and or which are under development.

Calibration kits to improve the reliability of impedance measurements at the nanoscale, as performed by end-users such as the academic community and the semiconductor industry will also be available shortly. Fabrication of calibration kits have been detailed and disseminated to large community of end-users through open access publication published during the project (conferences and paper accepted in peer-reviewed journals).

Impact on the metrology and scientific communities

The current development of capacitance and inductance standards enables traceability of impedance, permittivity and loss measurements to be established at the nanoscale. These advances will extend the measurement capabilities of the leading European NMI project partners in terms of the characterization of advanced materials such as ferro-electric, multi-ferroic, and piezoelectric-resistive materials important to the electronics industry. The project's multi-physics approach has already improved measurement capabilities and expertise of project partners involved in microwave component characterization and for the first time in Europe measurement devices operating under non 50 Ω conditions have been robustly investigated.

Research in the project on on-chip power measurements has created new power measurement detectors with capabilities based on the latest BICMOS 55 nm technology and the most advanced instrumentation is a world first. Using the latest fabrication processes based on project developed technologies has improved the experience of early users in both the industrial and academic sectors. These detectors have potential for exploitation by electronic component manufacturers engaged in 5G-product development because they are based on the latest ST Microelectronic technology. Detectors have been developed, manufactured and characterised: their performances (sensitivity, matching, and linearity) are excellent at 42 GHz. One of them is based on zero power consumption that is of great importance for energy saving devices.

Impact on relevant standards

Project progress and engagement was disseminated to IEC (TC 47, 49 and 113), ISO (TC206), IEEE (P1859/D6), VAMAS (TWA24) and EURAMET TC-EM SC-RF&MW/EMC, and SC-LF committee meetings. These reports describe the dissemination of good practice guides and the organisation of meetings dedicated to standardisation activities relating to semiconductor devices, piezoelectric and dielectric devices and characterisation of materials at the nanoscale. The consortium has also interacted with CEN/CENELEC/ETSI "Sector Forum Smart and Sustainable Cities and Communities" with a view to presenting the projects results to the appropriate CEN/CENELEC standards committee.

Longer-term economic, social and environmental impacts

The new traceability measurement capabilities for impedance developed in this project will aid the industrial competitiveness of European nanoscale measurement instrument manufacturers and supports the development of technical innovations in the ICT sector. Dissemination of improved characterisation methods for piezo and ferroelectric material under realistic in-service conditions will generate a European skills base that can support European electronics industry innovation and competitiveness. The new European power efficiency evaluation capabilities based on the multi-physics approach developed in this project, now enable

reliable evaluation of electronic component heating effects – an important step in future ICT product innovations.

6 List of publications

1. Bernd Kästner, Franko Schmähling, Andrea Hornemann, Georg Ulrich, Arne Hoehl, Mattias Kruskopf, Klaus Pierz, Markus B. Raschke, Gerd Wübbeler, and Clemens Elster, "Compressed sensing FTIR nano-spectroscopy and nano-imaging", Optic Express, April 2018, https://doi.org/10.1364/OE.26.018115.

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