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oordinator: <i>Djamel Allal, Dr., LNE</i> Tel: +33 1 30 69 21		50	E-mail: djamel.allal@Ine.fr	
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1 Overview

In February 2014, the European Electronic Leaders Group, representing the main companies in the sector, identified 3D integration of heterogeneous semiconductor technologies as the key opportunity for growth in Europe. 3D integration technology uses copper Through Silicon Vias (TSV) to electrically connect a stack of chips-bonded semiconductor wafers and dies to produce 3D stacked integrated circuits (3D-SICs) with an optimum combination of cost, functionality, performance and power consumption. This project has brought solutions to overcome the lack of traceable measurement tools and methods for reliability assessment of TSV-based 3D heterogeneous integration, by developing reference materials and calibrated standards and measurements, certified and tested, for the introduction of these 3D-SICs and enabling the progress of the electronics industry in Europe.

2 Need

While this technology is already used in imagers, memories and MEMS, its extension into new areas required a much larger density of higher aspect-ratio, smaller TSVs. This has created new metrological issues related to the dimensional and electrical characterisation of these TSVs and to the characterisation of heat caused by the higher current density in those structures.

Another aspect of this technological vision was that each function of the 3D stack samples (i.e. memory, sensor, biochip) can be manufactured independently at the right node (the node is the number representing the lowest size of the chip features) and in an optimised production line. 3D integration allowed them to be combined into a single compact system, with logic devices, memories, imagers and MEMS structures from different wafers (from various foundries) using different manufacturing processes. However, this introduced new traceability requirements in the metrology for 3D integration, as for instance for TSVs with a high aspect ratio which requires complete profile shape information. In fact, for this kind of TSV, any deviation from the targeted profile - such as undercut or bottom distortions or even high roughness or the non-conformity of the isolation of the barrier and seed layer was an important issue. An increase in the resistivity can be observed in TSVs having reduced dimensions and copper (Cu) having a small grain size and this needed accurate electrical nanoscale measurements.

3 Objectives

This project focuses on developing the traceable measurement capabilities for structural and chemical defects inspection in high aspect ratio through silicon vias (HAR TSV) and wafer/chip bonding and thinning. The JRP will also develop new accurate measurement techniques for thermal and electrical materials characterisation at the nanoscale of the TSVs with the following objectives;

- 1. To develop reliable 3D characterisation techniques, protocols and standards to accurately measure (at micron and submicron resolution) dimensional and structural properties of high aspect ratio (HAR>10) TSV interconnects before and after Cu filling: sidewall roughness, via shape, seed- and barrier-layer thickness, sidewall layer conformity, void detection and characterisation, grain size and grain boundary character distribution of the copper grains, crystalline structure, dislocations, stress around the TSV. In addition, for 3D-SICs with high density TSV interconnects, it is important to consider non-destructive wafer measurements as well as statistical data collection to enable the implementation of the measurement techniques in a production environment.
- 2. To develop methods to accurately measure the electrical and thermal transport properties of nanostructured copper TSV interconnects in order to establish traceable measurements of electrical conductivity and temperature change in copper as a function of the current density. Modelling of thermal transport in those structures will help to identify the various thermal scattering mechanisms in nanostructured copper grains.
- 3. To develop metrology tools, protocols and standards for high lateral and z resolution (sub microns for x-y, nm for z) non-destructive wafer to wafer alignment control before and after bonding as well as the characterisation of the bonding quality of wafers and dies: parameters at die level such as curvature, surface roughness and flatness which might need to be coupled with wafer level information; wafer/die contamination before bonding; wafer/die interface defectivity and adhesion after bonding; local stress and thermal dissipation at the interface of bonding wafers and dies will also be considered.



- 4. To provide traceable metrology for thickness uniformity control and for the surface quality of wafers/dies thinning (in the presence of circuits) and measurement techniques related to stress relaxation, crystalline defects and surface contamination.
- 5. To engage with the semiconductor industry and others to facilitate the take up of the technology and measurement infrastructure developed by the project, to support the development of new, innovative products utilising 3D-stacked ICs, thereby enhancing the competitiveness of EU industry.

4 Results

4.1 Objective 1: Reliable 3D characterisation techniques, protocols and standards to accurately measure dimensional and structural properties of high aspect ratio TSV interconnects before and after Cu filling

The aim was to accurately measure (at micron and submicron resolution) dimensional and structural properties of high aspect ratio (HAR>10) TSV interconnects before and after Cu filling. Such accurate measurement could be made possible thanks to the development of the first reliable 3D characterisation techniques (traceable AFM based methods, SEM and FIB/SEM techniques, TEM, IR microscopy and SAM, X-ray spectrometry, Raman spectroscopy and synchrotron based methods). The parameters to be measured were sidewall roughness, via shape, diameter, sidewall angle (top and bottom), via bottom profile (curvature), depth,-seed-and barrier-layer thickness, Cu pumping, sidewall layer conformity, void detection and characterisation, grain size and grain boundary character distribution of the copper grains, crystalline structure, dislocations, stress around TSV, post-CMP topography.

Physical modelling using Monte Carlo simulation and 3D modelling of the X-ray standing wave field will was performed to optimise SEM imaging and to adapt the GIXRF state of the art technique to 3D depth profiling, to probe both filled and non-filled TSVs.

Scanning electron microscopy (SEM) and focused ion beam-SEM techniques have been employed by PTB, CEA and FhG to characterise critical dimensions (CD) and Line-Edge Roughness respectively Line-Width Roughness (LER/LWR). Standard top view measurements deliver radius and roundness deviation of the TSVs, which could be verified by comparison of direct topography measurements by atomic force microscopy (AFM). After sample preparation, measurements on through silicon vias (TSV) cross sections were performed revealing regular roughness structures along sidewalls of TSV. While SEM images show a strong regularity. AFM profiles show a more random structure. SEM can be employed to quantitatively determine lateral geometric features such as pitch, width or diameters and line edge roughness to high precision. The geometry of a feature can be derived from SE (secondary electron) yield signals, because the SE signal is proportional to the cosine of the tilt angle of a surface and because the SE yield increases exponentially the closer the beam enters at the vicinity of a step. Cross sectional profiles of SE yield (averaged of 5 neighboring scan lines) versus lateral axes were used as basis to evaluate the edge positions along the circular border of the TSV. The set of all lateral positions of the edge transitions represents the circular shape of the top view of the TSV (red) to which a circle has been fitted (blue), as shown in Figure 1, with a radius of R = 1598.5 nm for this example. With AFM values of the TSV radius of around 1.6 µm could be confirmed with an uncertainty of 20 nm. The roundness error has been estimated to be 60 nm.



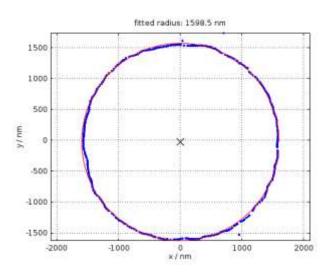


Figure 1. Circle fitted to lateral coordinates of edge transitions of the via sidewall.

SE-SEM is a technique optimally used to characterise the geometry and lateral roughness of the contour of edge transitions. Top views of TSV deliver precise diameter and roundness data.

The performances of optical techniques (full field interferometry, Confocal Chromatic and Time-Domain OCT (IR interferometry)) are compared with SEM measurements on various TSV diameters with 10µm depth. All techniques are providing similar results in depth. Each technique has advantages and limitations. The time Domain OCT based on a new generation LISE-HR sensor developed at Fogale demonstrated capability down to 10 µm of minimum depth and 3 µm of minimum diameter with no limitation in aspect ratio. White Light Vertical Scan Interferometry (VSI) could measure TSV depth down to 3µm wide in diameter with good matching vs SEM.

In Figure 2, a summary table is presented for six techniques evaluated for CD measurements in upper row and depth measurements in lower row. Different aspects are assessed such as throughput, measurement range, resolutions and dimensional type of output (scan or area). White light interferometry (WLI) is the more versatile technique for TSV dimensional characterisation.

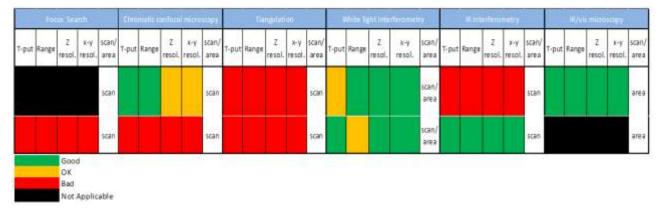


Figure 2. Benchmarking comparison between technologies for TSV CD and depth measurements.

3D-AFM has been used for non-destructive measurements of dimensional properties of TSVs. AFM usually applies conical or pyramidal shaped AFM tips. As a result, images generated by an AFM are the dilated result of the real structure by the tip geometry. Consequently, the steep sidewalls of micro and nanoholes cannot be properly measured by the conventional AFM technique, since the tip geometry prevents its contact with those regions. Therefore, the conventional AFM technique is not capable of measuring the TSVs dimensions directly due to almost vertical sidewall structures of TSVs. Of course it is possible to measure TSVs by conventional AFMs after TSVs are cleaved by e.g. Focused Ion Beam (FIB) devices. However, this is a time-consuming and destructive procedure.



To achieve true 3D measurements of dimensional properties of TSVs, a 3D-AFM has been further developed and optimised at PTB. The 3D-AFM uses flared tips. Such a tip has an extended geometry near its free end which enables the probing of steep and even undercut sidewalls of micro and nanoholes.

The difference between conventional AFMs and the 3D-AFM concerning the measurement strategy is that conventional AFMs usually measure in a scanning manner, well applicable for measuring e.g. surface textures, while in 3D-AFM measurements sample features are probed in a point-wise manner by an AFM tip approaching along a 3D vector path, which is typically given by the normal vector of the surface. Measurement points can be flexibly defined, for instance, to obtain high density points at areas of interests like a touch-trigger CMMs for 3D measurements at the nanoscale.

Three different measurement modes referred as "top-down imaging ", "sidewall probing" and "XY contour probing" have been developed. Measurement result of a TSV with a nominal diameter of 3 μ m using the "top-down imaging" mode is shown in Figure 3.

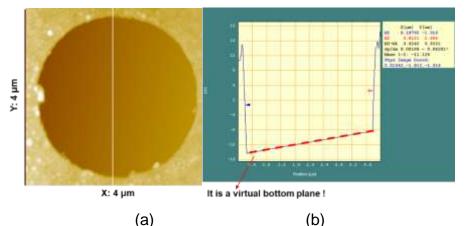


Figure 3. Measurement result of a TSV with a nominal diameter of 3 μm measured by the 3D-AFM in the top-down imaging mode, shown as (a) an AFM image and (b) a cross-sectional profile at the marked position.

To measure the sidewall profile of micro- and nanoholes, "sidewall probing" mode is applied. The measurement result is depicted in Figure 4. Using this mode, the sidewalls can be measured with high pixel density with reduced measurement time.

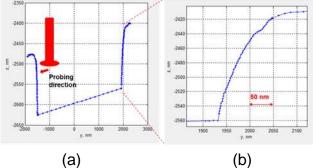


Figure 4. Measurement of sidewall profile of the TSV using the "sidewall probing" mode, shown as (a) a sidewall profile measured in the xz plane and (b) a zoomed-in view at the marked position.

To measure the roundness and diameter of micro- and nanoholes, the "XY contour probing" mode can be applied. Figure 5 shows the measurement result of the TSV using such mode.



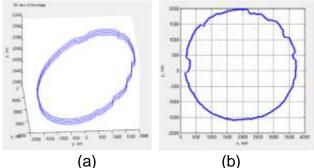


Figure 5. XY-contour measurement of the TSV using the "XY contour probing" mode, shown as (a) a 3D view and (b) an xy contour profile.

Traceability via metrological AFM can be established using a top-down approach (or optical interferometry approach) and a bottom-up approach (or crystal approach). In this project, we applied two traceability approaches in a joined manner for calibration capabilities.

One of the main concerns for Cu filled Through Si Vias (TSVs) processing is related to voids that remain present in the TSV after Cu plating. Various sizes and amounts of voids were shown to be present in TSVs, as shown in Figure 6.

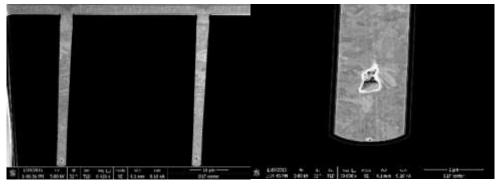


Figure 6. SEM images showing small voids near the TSV bottom at the centre of the wafer.

The presence of voids in Cu filled TSVs on a wafer is typically checked by making destructive local crosssections, for example using a focused ion beam (FIB) and SEM imaging. The potential of two different nondestructive techniques for TSV void detection was assessed in the 3D STACK project: scanning microwave microscopy (SMM) by LNE and METAS and GHz-scanning acoustic microscopy (GHz-SAM) by IMEC.

SMM combines the nanoscale spatial resolution of the AFM with the broadband electrical measurement capabilities of Vector Network Analyser (VNA). A microwave signal is sent directly from the VNA and transmitted through a resonant circuit to a conductive AFM probe that is in contact with a sample being scanned.

The SMM measures the complex reflection scattering parameter S_{11} . At the current time, studies on metallic and insulating substrates were reported that took advantage of the penetration ability of microwaves through materials. In these works, qualitative SMM imaging was performed exploiting the long-range electromagnetic (EM) interaction between microwaves and matter. Electrical contrast was obtained for metallic samples and the dependence of EM penetration depth on the applied frequency through the metallic skin effect was used as contrast mechanism.

In the case of a metallic sample, the electromagnetic waves in the range of microwaves have low penetration depth. Figure 7 shows the S11-amplitude (top) and S11-phase (bottom) maps simultaneously obtained with the AFM topography, at different VNA frequencies. The amplitude and phase maps show a contrast difference between Cu and SiO2, which indicates the different electrical properties for those materials. S11-amplitude (at 0.92 GHz and 3.60 GHz) and S11-phase (at 0.92 GHz and 5.44 GHz) maps show a contrast inversion



compared to results obtained at other frequencies. However, at this work frequencies range, these maps show non-evidence of the presence of voids.

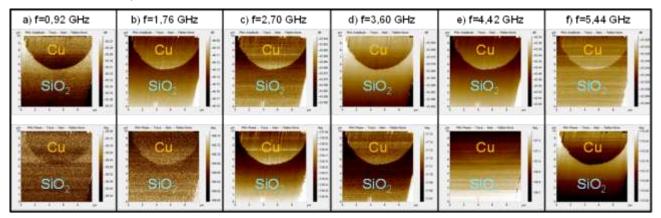


Figure 7. Influence of the frequency of the electromagnetic wave in SMM images. S11-amplitude (up) and S11-phase (down) maps for frequency values between 0.92 GHz and 5.44 GHz. Size: 10 μm x 10 μm.

Scanning acoustic microscopy is a well-known and commonly used technique to detect voids and delamination in microelectronics chip packages or in wafer-to-wafer bonding. Its resolution can be increased by increasing the frequency. In this project, a GHz-SAM system developed by PVA TePla was assessed for its use in microelectronics metrology, and especially for its potential to detect voids in TSVs.

Figure 8 shows SAM images from a Si chip, but taken with increasing sound frequencies. This clearly shows the impact of frequency on spatial resolution, and indicates that GHz-SAM is capable to detect features with resolutions of 1 μ m or even below. The experiments and tests performed within the project indicated that the technique has very promising features, but that it is not ready for implementation in the fab and for standardization. However, some important insights were gained which should be taken into account for future standardization.

GH2:TSV Fringes Study/TSV Fringes Study (New Tool Location)/ingrid (With Copper)/SeveralTSVs:TSV1_(1-03)GH2

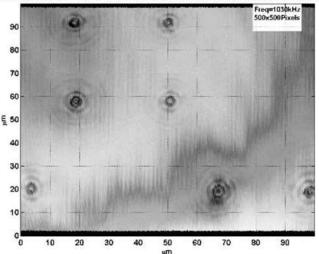


Figure 8. GHz-SAM scan on a sample with TSVs containing voids.

From measurement methodology point of view:

- It is important that the distance lens-focus is controlled and maintained during scanning as accurately as possible, to avoid the wide fringe issue. The exact error margin on this distance depends on the scan region and on the lens, and has to be assessed and provided by the instrumentation vendor. For this reason, it seems best to define the maximal allowed scan region for a certain system and a certain lens, for a certain application.



- Because of this wide fringe issue and small focus distance, it seems unlikely that scans can be made covering a full wafer using the GHz-SAM. The best implementation would be a combination of a wafer-level scanning system, as is already existing, with a GHz-SAM lens which can be used to look into detail at some regions.

- A good control of the distance lens-sample surface is also required to enable an optimal measurement of the Rayleigh fringes. The lens dimensions and parameters should also be optimised to get more focused and detailed Rayleigh fringes.

- A good synchronization of the motor of the scanner and the microcontroller of the trigger unit is required to avoid jitter of the images.

- GHz-SAM is very sensitive for particles at the surface. They should be avoided when using the tool to test TSVs.

From a metrology point of view:

- The detection of TSV voids by GHz-SAM was not proven yet. We are confident that voids can be detected, but this has to be further assessed when an optimized and stable instrument is available.

- The visualization of Rayleigh fringes by GHz-SAM will allow detecting > 18 nm wide cracks or discontinuities in the Si surface. This could also help to detect sidewall delamination of the TSV.

- The visualization of Rayleigh fringes by GHz-SAM will allow detecting large stress fields. From our experiments, we learned that the effect on the fringes is small for stress fields around a TSV (~ 100 MPa). For this application, the technique might be too complicated compared to existing techniques (ex. Raman spectroscopy, polariscopy). For higher stress fields, especially in materials that cannot be investigated using these existing techniques, this technique might offer a unique new metrology solution. But more research is required to confirm this.

- GHz SAM is very sensitive to surface and sub-surface defects. It can most likely also be used for that purpose as metrology tool. This might be a new application, which has to be investigated in more detail.

In summary, dimensional and structural properties of high aspect ratio TSV interconnects were implemented, before and after Cu filling using both destructive and non-destructive techniques. Even if some techniques have had their efficacy not fully demontrated like GHz-SAM and SMM, the objective can be considered to be achieved in terms of the different parameters that had to be characterised for all techniques combined.

4.2 Objective 2: Methods to accurately measure the electrical and thermal transport properties of nanostructured copper TSV interconnects

The aim was to focus on the development of methods to accurately measure electrical and thermal transport properties of nanostructured copper TSV interconnects in order to establish traceable local measurements of electrical conductivity and temperature change in copper as a function of the current density. The modelling of thermal transport in these structures was performed in order to identify the various thermal scattering mechanisms in nanostructured copper grains.

Scanning Thermal Microscopy (SThM) was used by CMI in different configurations and for different samples, trying to get maximum out of the technique possibilities, and presenting ways how to make it traceable. It should be noted that despite the fact that SThM has unprecedented capability in spatial resolution of temperature and thermal quantities, it is not the most accurate technique if we want to get the absolute thermal quantities values. For many situations, more conventional techniques with lower spatial resolution, but with simpler traceability chain can be used. This might also be the case of some of the TSV systems used during the project that consist of relatively large structures, where the ultimate spatial resolution of SThM is not fully employed anyway.

To compare the results with a sample that would be much simpler, but completely known, to be used in the experimental techniques development and data processing algorithms debugging, a simple test sample was created, consisting of a single gold wire (30 micrometers diameter) in a polymer matrix. Top and bottom of the sample were polished and coated by gold film to deliver power to the wire. Schematic of the sample is shown in Figure 9.



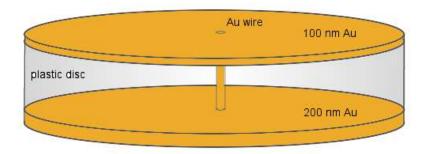


Figure 9. Schematics of the CMI test sample: gold wire in polymer matrix.

Most of the measurements were performed in the single probe SThM configuration, which is the default and the only commercially available SThM regime. The probe is either used as a temperature sensor, minimising its self-heating and measuring the probe resistance, or used as a thermal conductivity sensor, heating it significantly by electrical current passing through it and monitoring the heat losses to the sample.

A two probe SThM system was also set up to be able to pass the heat flow from one surface location to another in a more controlled way. This has no practical use in the power dissipation measurements that were a primary goal of this study; however it illustrates the sensitivity of the SThM to local temperature and to surface and subsurface material distribution. In the two probe system we are able to control two independent probes, one formed by doped silicon and second one by a resistive element. We can position and approach the probes to any position on the sample, control which probe is heated and which is sensing temperature and move one of the probes.

A sensitivity analysis, related methodology and an uncertainty budget for SThM local temperature measurements was carried out. The uncertainties are significantly dependent on the particular sample and its geometry. In particular, even if the heat is generated very locally in the sample (e.g. on some defect within the TSV), the temperature distribution on the surface is highly affected by the distribution of materials in the sample and their thermal conductivity and for many possible geometries the surface temperature variations can be almost negligible.

Results on local thermal conductivity measurements are presented here. The local thermal conductivity affects both the SThM sensitivity and the local temperature distribution, so even if we are interested in local dissipated power, it is an important quantity. In Figure 10, examples of measurements in the thermal conductivity contrast mode are shown, both for copper covered and uncovered (polished) samples. While on polished samples we can see some conductivity contrast at the TSV location and around it, this is not the case of the copper covered sample. In general, the thermal conductivity values of the materials used here (silicon, copper) are not very suitable for SThM measurements as the method is most sensitive for much smaller thermal conductivities. That is the reason why we did not evaluate the local thermal conductivity (the uncertainty would be in tens of percents at least) and we have used the technique only to show the potential defects in TSVs.



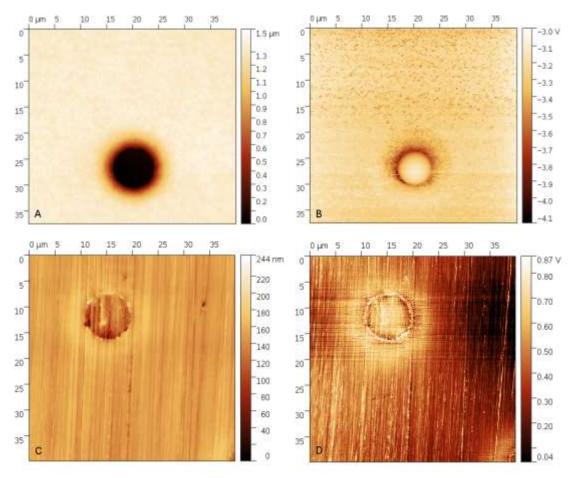


Figure 10. Local thermal conductivity contrast on TSVs: (A, B) topography and thermal signal on copper coated TSV sample, (C, D) topography and thermal signal on polished TSV sample.

The two probe setup has also been tested to see how the in-plane thermal conductivity can be measured on such samples. The measurement shown in Figure 11 shows that the two-probe SThM can be used to obtain the local information about the in-plane conductivity, however the contrast is not very high. This is common to all the SThM techniques while measuring on high thermal conductivity materials. Therefore the results of the two probe measurements are not significantly better than single probe measurements. If one needs to get in-plane and out of plane conductivity, combination of the two approaches would be still needed, however for routine inspection of defects the two probe method is too complex to handle.

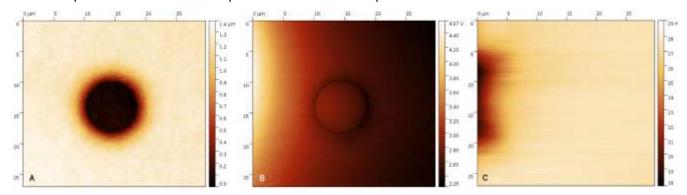


Figure 11. Two probe SThM measurement on the copper coated TSV sample: A) topography, B) moving probe SThM signal (heat sink), C) fixed probe SThM signal (heat source).



The local temperature measurements were performed on a special sample suitable for bonding. The bottom side of the sample was connected via conductive paste. A current stabilised power supply was used to feed the system by current in the range of 0-40 mA. The sample structures were too big for conventional measurements. As a first step we have performed measurements at single spots, at different distance from the active TSV, assuming that we should observe a temperature gradient across the sample.

A typical result is shown in Figure 12. We can see that even if there is a clear temperature gradient while approaching to the TSV, there is a plenty of signal even at a half millimeter distance.

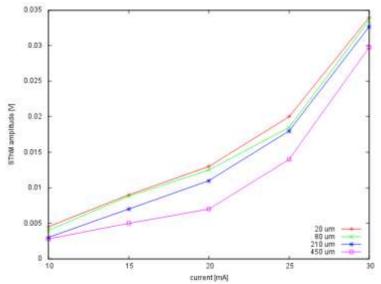


Figure 12. SThM signal difference for on/off TSV current (10-30 mA) for different distances between the TSV position and SThM probe location. The maximum amplitude of the thermal signal corresponds to 0.1 K temperature difference.

Data interpretation from the SThM measurements, in terms of the local power dissipation, is not straightforward. One needs to take into account the local material distribution and local thermal conductivities, which can cause large spread of the temperature field in the sample. SThM is sensitive to measure even this, however data interpretation then needs a lot of knowledge about the sample. Even if the absolute temperature measurements using the most complex case (unknown sample and probe) have uncertainty in order of Kelvins, the sensitivity of the method is in miliKelvin range. If the measurement of the temperature distribution is performed within a single scan, thus reducing most of the uncertainty components related to probe and to probe-sample contact, uncertainty can be much lower. In this way the desired uncertainty is achieved.

From the point of sample geometry, the biggest problem is that we want to monitor the power dissipated in TSV, which means that the TSV should be connected via wires or vias with lower electrical resistance. This however means typically also lower thermal resistance and the vias act as a heat sink. This might be good for the device performance, but for the measurement technique it is an unwanted effect.

To date, most of the advances in the SMM technique were achieved studying surface structures including undoped and doped semiconductor materials. Electrical resistivity measurements of metal materials have not been reported using the SMM technique. Only qualitative S_{11} contrasts could be obtained, which allow distinguishing two different regions, which correspond to the Cu TSV top surface and the silicon substrate.

A correct calibration of the SMM instrument would also show a contrast difference in the resistance and capacitance maps, both obtained from conversion of the S_{11} raw data. However, this calibration step is not possible because the resistivity values that we expect are outside of the range of resistivity values allowed by SMM technique. The Cu TSV resistance (a few tens of m Ω) is masked by the noise floor (resistance differences that could be distinguished using the SMM technique cannot be smaller than 20 Ω).

We conclude that, the SMM technique is not adapted for electrical resistivity measurements of metal materials and the correlation of the SMM measurements to detect grain boundaries with grain size distribution becomes difficult.



METAS modified their SMM in order to not employ high frequency signals for the measurements, but rather measure in the direct current (dc) regime. The VNA was therefore disconnected and the measurement setup was installed using a power supply to generate a constant voltage and a voltmeter to measure the voltage drop across the TSV which is probed by the microscope tip.

To conduct these measurements additional sample preparation is necessary. To close the electric circuit the wafer is glued with conducting silverpaste to a sample holder which is then connected with a Cu wire together with the voltage source and voltmeter used. Unfortunately, the measured voltages did not allow any conclusion about the TSV resistivity which was fully masked by the noise floor.

Reasons for this negative result are on the one hand the low expected resistance of a single TSV which in itself is a challenge to detect. To solve this, a different measurement setup might lead to better results. A possible suggestion is to employ a lock-in amplifier and measure small currents through the TSV instead of dc voltages. Finding a suitable alternative setup however is expected to be too time consuming and is thus beyond the scope of the project. Another reason is oxidation of the Cu leading to bad electric contacts between tip and TSV and also between TSV and silver paste. A possible route around this could be more elaborate sample preparation using additional etching steps immediately before applying the silver paste to avoid building up of the oxide layer.

Another use of the SMM technique was the investigation of grain boundaries. A set of measurements at 45.1 GHz obtained on a mechanically polished wafer are shown in Figure 13.

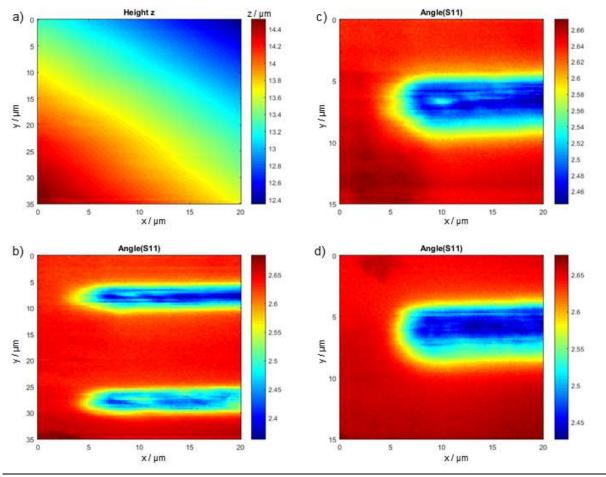


Figure 13. Measurements of the mechanically polished TSV cross sections provided by IMEC. In a) the topography corresponding to the S11 phase measurement shown in b). In c) and d) higher resolution scans of the top and bottom TSV are shown.

In Figure 13b two neighboring TSVs are depicted by plotting the phase of the microwave reflection S_{11} in degrees. The TSVs are along the x-axis with spacing along y of 20 μ m and visible diameter of 5 μ m. The homogeneous red signal corresponds to the Si host wafer while the blue/turquoise signal is caused by the



TSVs giving an overall contrast around 0.25° between Si wafer and Cu TSV making the two materials well distinguishable. To exclude topography as a possible source of the described contrast, Figure 13a shows the corresponding height map indicating a planar polish with a slight tilt which is most probably also the reason for the different lengths of the two TSVs. Having verified the SMM's ability to measure a clear contrast between TSV and host wafer in the next step its ability to detect grain boundaries and seed and barrier layers. Therefore Figures 13c and 13d show higher resolution scans of the top and bottom TSV.

In c) and d) a sub-micron thin transition region between TSV and wafer can be identified all around. This is where seed and barrier layer are to be expected, the data however does not allow conclusion about resolving these two layers. Supposedly the resolution of the SMM and the electrical contrast between these layers is too low to unambiguously detect them.

Also detection of grain boundaries in the Cu does not seem to be possible in this sample. There are inhomogeneities in the Phase of S_{11} but they are much larger than the expected grain size, which are expected to be around 400 nm. We identify two reasons for not being able to resolve these grains. First is the mechanical polishing to expose the cross sections. Since Cu is a very ductile material smearing out the grains in the course of the polishing is to be expected if the process parameters are not perfectly adjusted. Another reason is that the electrical properties of the different grains are not different enough to be within reach of the SMM's sensitivity. To take these difficulties into account a different set of samples has been investigated to further analyse the grain boundaries.

Figure 14a shows the resistance map obtained by LNE with a C-AFM (Resiscope) represented in logarithmic scale for a best visualization. A profile along the Cu TVS long axis is extracted and showed in the Figure 14b. The resistance values are represented in normal scale with a maximum resistance variation of 17 k Ω .

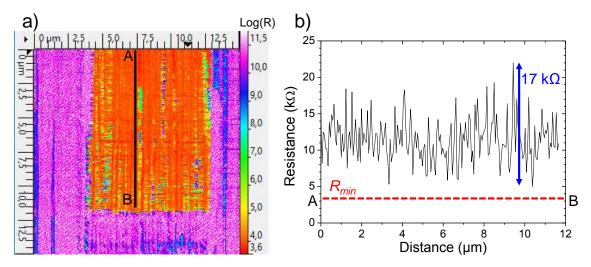


Figure 14. a) Resistance map of the Cu filled TSV F (10 μm x 120μm, no voids), 15 μm x 15 μm. b) Resistance profile in normal scale.

Unfortunately, the copper resistivity in TSV could not be determined due to technical limitations of the Resiscope system and some experimental constraints as the influence of the aging time of copper surface exposed to moist air.

In summary, different techniques were implemented in order to measure the electrical (SMM, C-AFM) and thermal transport properties (SThM) of nanostructured copper TSV interconnects in order to establish traceable measurements of electrical conductivity and temperature change in copper as a function of the current density. Modelling of thermal transport in those structures has been performed to help to identify the various thermal scattering mechanisms in nanostructured copper grains. Unluckily this objective was not fully achieved considering the limit of the implemented electrical techniques to characterise a high electrical conductivity such as copper in microscale dimensions.

4.3 Objective 3: Metrology tools, protocols and standards for high lateral and z resolution



non-destructive wafer to wafer alignment and bonding quality control

The aim was to develop metrology tools, protocols and standards for high lateral and z resolution (sub microns for x-y, nm for z) non-destructive wafer to wafer alignment control before and after bonding as well as the characterisation of the bonding quality of wafers and dies.

The wafer bonding process is a critical step for 3D technology, and one of the key associated metrology steps is the wafer-to-wafer or die-to-wafer overlay measurement. After bonding, controlling misalignment with various thick material stacks, through silicon, requires using light in the IR domain. 3D interconnect dimensions are being scaled to lower levels, with pitches of 5µm and below. For further scaling down, wafer-to-wafer overlay alignment of 400 nm is required and expected to reduce even further to 200 nm.

Two different techniques have been used to measure overlay on a bonded wafer: CEA and Fogale used IR microscopy and IMEC used laser-scanning IR.

With IR microscopy, image acquisition was done by a 50X objective providing a maximum lateral resolution of 0.2µm per pixel and about 0.5µm optical resolution. The bonded wafer available for this study is made of a Si wafer directly bonded on a glass wafer. The wafer was illuminated from its backside with IR source and the optical setup collecting light passing through the wafer was positioned at the wafer frontside. Figure 15 shows the design of the overlay targets processed at two levels (one in each wafer) and used for the overlay measurement.

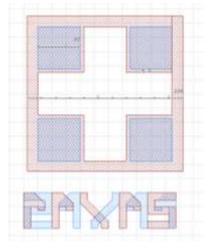


Figure 15. Overlay targets of the Si/glass bonded wafer.

We can notice that these targets are positioned in a dedicated wafer area free of metal structures that would prevent the IR light to pass through. The 50X objective was used to obtain the optimum field of view (FOV) showing a full image of the target. As observed in Figure 16, the two levels, one per wafer, are separated by approximately 130µm and were not in focus at the same focal position due to limited depth of focus for this objective.

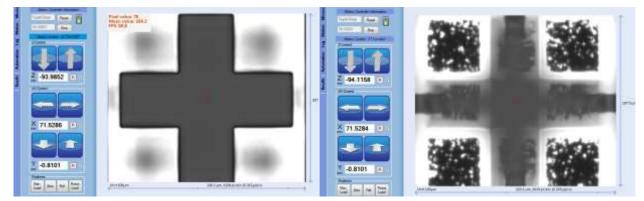


Figure 16. TMAP results from the CEA sample. With Si wafer up and IR illumination from glass wafer side. Target focused images obtained on TMAP using 50X objective (upper level to the right and lower level to the left).



As the standard microscopy used on this tool did not provided in focus images of the two targets simultaneously, an envisioned workaround was to use dual microscopy allowing imaging from both wafer front and backside with independent focal points. According to the supplier, dual microscopy was not necessary, as a double image grabbing at different focus points would be technically possible. However, as the on-tool software was not ready to be used for this application, it was not possible to obtain a direct overlay measurement.

Laser-scanning IR microscopy, used in this project is based on confocal IR laser scanning microscopy. To check alignment, typically IR pictures are taken at the bottom left and top right of the sample, i.e. at the position of dedicated alignment markers. Alignment structures such as Vernier structures, crosses and circles are then analysed using a Matlab script to check the alignment.

The current limitation of this technique is that for die-to-wafer inspection, measuring a full wafer is very time consuming (about 2 working days). At best the interface, i.e. the structures of top and bottom wafer, should be within the depth of focus of the used objective lens, as was also mentioned for the IR microscope above. A higher magnification increases spatial resolution, but decreases this depth of focus in general (higher numerical aperture). When the distance between the two bonded surfaces is smaller than the focal depth, the system can easily be used for alignment. If this is not the case, two images have to be taken, one at focus for each wafer interface, and combined to check alignment, which can introduce additional failures.

Another option is to perform 3D-measurements, with automatic scanning along Z. However, this is time consuming and requires good operator skills. Figure 17 shows two wafer-level alignment measurement results obtained on a bonded wafer. The bonding accuracy requirement had to be better than 2 µm. 66 dies/wafer were measured. The ones within spec are indicated in green. The results show that the technique can be used for checking alignment, but as it is a manual system, it is too slow for in-line testing.

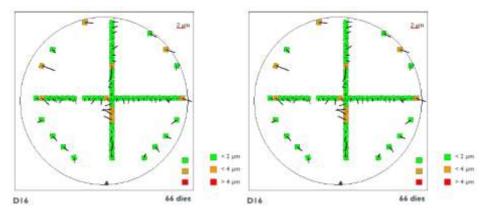


Figure 17. Examples of alignment result on the imec-sample obtained using Laser-scanning IR microscopy.

A High speed metrological large range atomic force microscopy system has been developed as a metrology facilitiy for 3D areal measurements for supporting 3D integration.

Atomic force microscopes (AFM) are widely applied for measurements of nanostructures and ultra precision surfaces for quality assurance in various nanomanufacturing industries including, for instance semiconductor, nano-optics and precision engineering. Earlier AFMs are applied mainly for imaging purposes. Tube scanners are usually applied in these AFMs and the voltages applied to the scanners are used to derive AFM images. Consequently the measurement results suffer from the shortcomings of the piezo actuators, such as creep and nonlinearity. The known bow effect of the tube scanners also leads to form errors in profile measurements. To solve this challenge, a number of metrological AFMs have been developed at NMIs worldwide. Compared to conventional AFMs, the metrology AFMs are typically equipped with laser interferometers for measuring the scanner's motion. In such a way, the displacement measurements performed by metrological AFMs are closely linked to the definition of the metre (direct traceability). Several international comparisons indicated that the step height calibration can be achieved with an expanded uncertainty (k=2) below 1 nm, and pitch calibration can be performed with a relative expanded uncertainty (k=2) below 2 x 10-5 today. The AFM technique has advantages of a high lateral resolution (down to a few nanometers defined by the tip geometry) and a high lateral resolution (subnanometer), non-destructive measurement capability. Furthermore, unlike optical techniques that are sensitive to material heterogeneity of the surfaces as mentioned above, the AFM technique is capable of offering high precision topography measurement results on surfaces of heterogenous materials.



These advantages make the AFM technique a highly potential technique for reference metrology of areal surface topography to solve the challenges mentioned above.

Unfortunately, there are several critical limiting issues. Firstly, the scan range of a conventional AFM is small, typically tens of micrometres. Secondly, the scanning speed of AFMs is usually very low, typically tens of µm/s. It not only leads to a very low measurement throughput, but also suffers from remarkable measurement drift due to the long measurement time needed. Some high speed AFMs are available today, however, they are mainly applied in bioscience for dynamic visualisation of nanostructures and their metrology performance is not required for such applications.

To overcome these limiting issues, in the frame of this project a high speed metrological large range AFM which is capable of highly accurate and large range measurements of surfaces and nanostructures has been further developed by PTB, optimised and applied for traceable 3D areal surface measurements of wafers for supporting the 3D integration. The instrument is based on a large range mechanical stage referred to as a nanopositioning and nanomeasuring machine (NMM).

Several important design concepts have been implemented to realise both, high measurement speed and high metrology performance i.e. in terms of sensitivity, stability, accuracy and traceability:

- the contact AFM mode is applied instead of the intermittent and non-contact modes, which offers shorter AFM response time and larger AFM sensing range, than the amplitude modulation (AM) mode.

- during measurements, the sample is scanned in the xy-plane solely by the NMM (such a motion usually has a constant velocity; therefore, high dynamics of the xy-scanner is not needed.), however, a high dynamic z-motion of the sample is realised by a combined piezo stage and the z-stage of the NMM controlled in parallel.

- the AFM output signal is combined with the position readouts of the piezo stage and the NMM to derive the surface topography. The combination of these readouts offers a large bandwidth of measurement signals, thus provides high-speed measurement capability.

- two important means are taken to reduce the distortion in measured profiles, namely (a) the time delay of sensor signals is corrected; (b) the position sensors of the AFM and piezo stage are traceably calibrated to the z-interferometer of the NMM in situ.

To demonstrate the metrology performance of the high speed Met.LR-AFM, Figure 18(a) shows a same surface profile measured at different speeds (from 10 μ m/s up to 500 μ m/s). It can be seen that the quality of measured surface profile is very similar despite the scanning speed has been increased by 50 times.

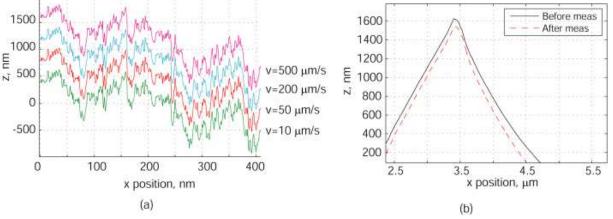
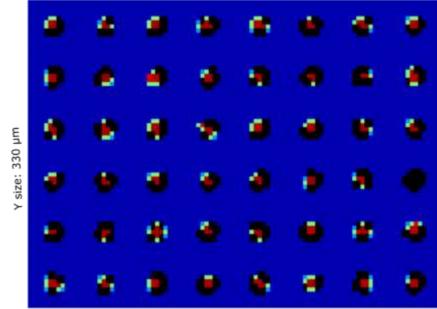


Figure 18. Surface profiles taken on a PTB roughness standard (RN 505) by the high-speed Met. LR-AFM, measured at the same location with different speeds from 10 μ m/s up to 500 μ m/s; (b) Tip shape characterised before and after measurements. Profiles are intentionally shifted along the y-axis for clarity;

Measurement of Bumps (solder is in the form of bumps when applied at the wafer level) of TSVs has been carried out by METAS as an application demonstration of WLI for 3D integration. As a first experiment, a dice with SnAg Bumps has been measured as shown in Figure 19. The result shows that the wafer surface can be measured with very high precision but there are many missing pixels in the area of the bumps. This is because of the surface angle. If it is too big the light is not reflected back into the lens and the result is a missing pixel.

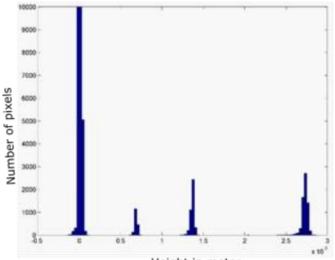




X size: 440 µm

Figure 19. White Light Interferometer image of the FhG sample with 5um Cu and 20 um SnAg and 55um pitch. The wafer surface is well depicted but there are many missing pixels in the bump areas.

The histogram of this image shows 4 groups of pixel heights in Figure 20. The first group is the wafer surface and it has a standard deviation of approximately 20nm. The second and third groups are most likely artefacts from the evaluation software of the instrument. The most likely explanation is that these are pixels which are very weak because the surface for these pixels has a too strong angle and little light is reflected into the lens. The fourth group is the bump height (approximately 27.5 um) and it has a standard deviation of about 15 um. The big standard deviation can be explained by pixels which are close to the bump peak and still have a small enough angle to give a relatively reliable result. Additionally, the bump height is most probably not completely uniform but this is expected to be not the main cause of the large standard deviation.



Height in meter

Figure 20. Histogram of FhG wafer depicted in Figure 19. The two middle peaks are software artefacts and the other peaks represent wafer surface and bump top.

The extraction of the bump shape as shown in Figure 21 is done with an algorithm which relies on a regular grid of bumps. This makes it possible to "cover" the holes which are visible in Figure 19. The algorithm consists of the following steps:

1: A plane is subtracted from the measurement data such that only minimal positive heights remain.

14IND07 3D Stack



2: A 2D Fast Fourier Transform (FFT) of this data is computed. The directions and distances between the bumps are taken from the 5 highest peaks in the FFT data.

- 3: Again the data from step 1 is taken and height limited such that only the wafer surface is visible.
- 4: The data from step 3 is filtered with a Gaussian filter.
- 5: The local maxima of the filtered data represent the centers of the bumps.
- 6: A plane can be fitted to the difference between the centers from step 5 and the centers from step 2.
- 7: The plane height can be minimized by adjusting frequencies and phase from step 2.

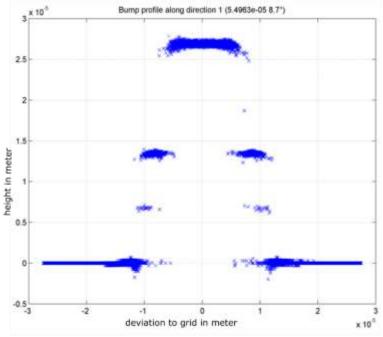


Figure 21. Height profile of a Bump of the FhG SnAg 20um sample.

In summary, several metrology tools have been implemented for high lateral and z resolution non-destructive wafer to wafer alignment control before and after bonding. The characterisation of the bonding quality of wafers and dies has also been performed. Considering the list of parameters that have been assessed thanks to such tools, this objective is achieved.

4.4 Objective 4: Traceable metrology for thickness uniformity control and for the surface quality of wafers/dies thinning

The aim was to provide a traceable metrology for thickness uniformity control and for the surface quality of wafers/dies thinning (in the presence of circuits) and measurement techniques related to stress relaxation, crystalline defects and surface contamination.

To characterise the cleanliness of the surface before and after the bonding, Total Reflection X-ray Fluorescence (TXRF) uses extremely low-angle X-ray excitation of a reflecting sample carrier surface, e.g. a silicon wafer in order to determine the mass depositions of surface contaminants. The incident angle of the x-ray beam is chosen to be below the critical angle for total external reflection at the substrate and thus limits the excitation to the outermost surface of the sample resulting in very low substrate related spectral backgrounds. The fluorescence signal emitted from the sample is characteristic of the present elemental contaminants.

Figure 22 shows the experimental set-up that has been used for the Total Reflection X-ray Fluorescence Measurements (TXRF). The total reflection geometry ensures very high sensitivity due to the reduced scattering background and the high solid angle of detection.



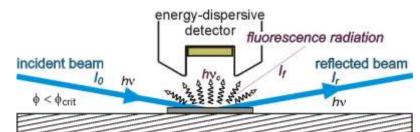


Figure 22. Experimental set-up for TXRF-NEXAFS experiments. Total reflection geometry ensures low scattering background and high solid angle of detection.

In TXRF and Grazing Incidence XRF (GIXRF), the incident angle between X-ray beam and sample surface is varied around the critical angle for total external reflection. On flat samples, the interference between the incoming and the reflected beam results in the so called X-ray Standing Wave (XSW) field. The intensity distribution inside the XSW strongly depends on the incident angle and can significantly enhance the emitted fluorescence intensity of an atom inside the XSW as well as reduce the substrate contribution simultaneously. In contrast to conventional TXRF, where the angle of incidence is fixed usually at 70 % of the critical angle, the GIXRF technique can take advantage of the XSW effect by performing angular scans around the critical angle to provide additional information about the depth distribution of the mass deposited on the substrate. The fluorescence signal of nanoparticles, thin layers and implantation profiles show different angular dependencies, which enables elemental depth profiling by GIXRF.

X-Ray Fluorescence analysis (XRF) in general is a highly sensitive technique to determine elemental compositions and mass depositions. In particular, XRF in grazing incidence geometry allows for very low limits of detection. However, the standard quantification methods of XRF rely on reference materials or calibration standards in order to compensate for missing instrumental information. As the spatial matrix elemental distribution of the calibration samples has to be as similar as possible to the specimens to be analyzed, their availability is very limited compared to the quickly growing amount of scientifically and technologically relevant material systems at the nanoscale.

This growing discrepancy between technological advances and metrological characterisation as well as validation capabilities can be addressed with the reference-free X-ray fluorescence spectrometry methodologies of PTB. By relying on radiometrically calibrated instrumentation and knowledge of the atomic fundamental parameters, no reference or calibration standards are needed for a quantitative analysis of the mass deposition of an element of interest.

The quantitative analysis in reference-free GIXRF is based on the Sherman equation, which provides the connection between the present mass deposition per unit area of an element with the measured fluorescence intensities for that element.

Vapour phase decomposition inductively coupled plasma mass spectrometry (VPD-ICPMS) starts with the vapor phase decomposition sample preparation technique by which any trace contaminants on the surface of a silicon wafer are collected into a droplet of liquid to be analyzed by ICPMS. The silicon wafer is exposed to hydrofluoric acid vapor in a sealed chilling chamber, which then forms a condensate on the wafer surface. This condensate etches the oxide layer off of the wafer surface along with any of the metal contaminants that are present on the surface. The condensate is then collected by rolling a drop of scan solution (generally a dilute mixture of hydrogen peroxide, nitric acid, and hydrofluoric acid) across the surface of the wafer. The drop is transferred from the wafer surface into a clean sample vial which is then analyzed for trace metals using ICPMS. This technique is capable of measuring metallic contaminants at concentrations ranging from 1E6 to 1E14 atoms/cm2.

The setup for reference-free GIXRF at PTB employs radiometrically calibrated instrumentation and an atomic fundamental parameter (FP) based reference-free quantification approach. An ultrahigh-vacuum (UHV) chamber**Error! Reference source not found.** equipped with a 9-axis manipulator was employed used for the measurements allowing for very precise sample alignments in all relevant degrees of freedom. The incident angle θ between X-ray beam and sample surface can be varied from -5° to up to 110° with a resolution of 0.0005°, which is sufficient for the GIXRF experiments. Additional photodiodes on a 2 θ axis allow for X-ray reflectometry simultaneously with the GIXRF measurements. For the detection of the emitted fluorescence radiation, a silicon drift detector (SDD), calibrated with respect to its detector response functions and detection efficiency was used. The incident photon flux was monitored by calibrated photodiodes. A sketch of the set-up is shown in Figure 23.



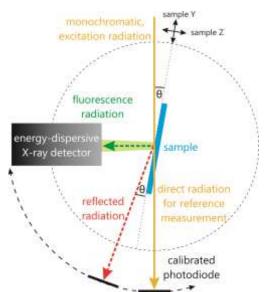


Figure 23. Sketch of the experimental GIXRF set-up in PTB's UHV chamber.

Setup for TXRF at CEA allows the use of 3 X-ray excitation beams such as:

beam 1 (W-Ma @ 1.77keV) to analyze Na, Mg, Al. The calibration is performed on Al response.

beam 2 (W-L β @ 9.67keV) to analyze elements from P to Zn notably. The calibration is performed on Ni response.

beam 3 (W « background » @ 24keV) to address heavier metals (Zr, Mo, Ta, W, Au, Pt...). This analysis beam is calibrated on Mo response.

In well controlled conditions, the TXRF measurement uncertainties (due to repeatability, reproducibility) were determined from uniform contamination on the wafer surface. These uncertainties (CI of 96%) are, for contaminants levels 100 times higher than detection limits, better than 15% for AI and Ni and 35% for Mo.

The spot size (few cm²) is defined by the detector characteristics. An exclusion edge of 15mm and 25mm respectively for beams 1-2 and beam 3 is used.

Direct TXRF analysis mode was performed on 5 points on the wafer with a time acquisition of 50 s per point for beam 2 and beam 3 and 100 s for beam 1 except for slots 5 and 7, 100 s for each beam. The coordinates of these points are (0,0);(0,30);(-30,0);(0,-30).

VPD-ICPMS or VPD-DC-ICPMS (HF Vapor Phase Decomposition-Droplet Collection – Inductively Coupled Plasma Mass Spectrometry) was performed using an automatic VPD tool (Rigaku VEE300) using a diluted HF/H2O2 chemistry as droplet collection and for analysis an Agilent ICPMS7500cs. The automatic droplet scan allows us to address a defined wafer surface). Then, the collection solution is manually transferred for metal contaminants quantification by using the ICPMS analysis.

Because VPD-ICPMS is destructive for the wafer (chemical collection step), VPD-ICPMS has been performed on similar purposely contaminated wafers in order to obtain reference data for the delivered ones. Indeed, VPD-ICPMS can be considered as a reference analysis since this one is calibrated from certified standard solutions and collection efficiencies of metallic contaminants are better than 98% for Al, Ni and Mo. Consequently, the analysis is very accurate (typically better than $\pm 15\%$ on $\geq E10$ at/cm²) and very sensitive (able to reach few E+7 at/cm² for some elements).

A comparison of TXRF results from CEA and PTB has been carried out. The following samples were produced at CEA by spin coating. The contaminants selected for all delivered wafers have been AI, Ni and Mo since these metals are usual calibration elements of TXRF using W anode excitation source. A previous wet cleaning were performed on wafers by using a standard diluted HCI/O3 cleaning recipe.



The spin coat/dry method is based on the deposition of a defined volume of an acidic solution spiked with a controlled contaminant concentration to cover the entire surface. After a fixed contact time, the solution is removed by spin drying leading to leave adsorbed ions on the whole wafer surface. Intentional contamination with Al, Ni and Mo has been performed by this way with a good uniformity and repeatability. The samples are described in more detail in Table 1. Slots 1, 5, 9, 13, 17 were analyzed by TXRF and sent to PTB and slots 3, 7, 11, 15, 19 were measured by TXRF and then by VPD-ICPMS.

At PTB, TXRF experiments were carried out using different incident photon energies of 1.622 keV, 2.5 keV and 9.5 keV, whereas at CEA, 1.77 keV, 9.67keV and 24 keV photons were used for the analysis of Al, Ni and Mo respectively. The PTB experiments were carried out the PGMError! Reference source not found. and the FCM beamlineError! Reference source not found. at BESSY II using the previously described setup. The CEA experiments were performed with an industrial TXRF (Rigaku TXRF Fab300) using two monochromator crystals and followed protocols defined by the tool supplier for this industrial tool.

Slot number	Analysis method	Contamination target /At./cm ²
slot 1	TXRF 5pts	clean reference
slot 3	TXRF 5pts	clean reference
	VPD-ICPMS	
slot 5	TXRF 5pts	E11
slot 7	TXRF 5pts	E11
	VPD-ICPMS	
slot 9	TXRF 5pts	E12
slot 11	TXRF 5pts	E12
	VPD-ICPMS	
slot 13	TXRF 5pts	E13
slot 15	TXRF 5pts	E13
	VPD-ICPMS	
slot 17	TXRF 5pts	E14
slot 19	TXRF 5pts	E14

Table 1: Sample description for the comparison experiments between PTB and CEA.

At PTB, the X-ray fluorescence spectra, recorded for each incident angle, are deconvolved using the known detector response functions for the relevant fluorescence lines as well as for relevant background contributions.

At CEA, the spectra are recorded at fixed angle (0.5°; 0.08° and 0.05° respectively for Al, Ni and Mo analysis). Spectra are processed with using deconvolution implemented on the Rigaku TXRF Fab300 software and calibration performed on the Al, Ni and Mo contaminated standard wafers (home-made wafers referenced to VPD ICPMS measurement).



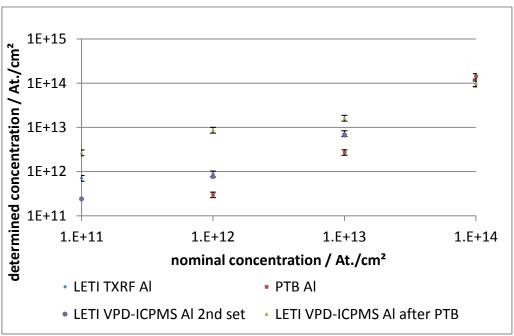


Figure 24. Comparison of the quantification results for Al.

In Figure 24, a comparison of the different quantification results for AI is shown. Even though the different tools results show a similar trend, the overall agreement is rather poor, especially at lower levels. For none of the samples analysed with the reference-free TXRF methodology of PTB reproduces either the LETI TXRF or the LETI VPD-ICPMS quantification result. However, one can notice that at E14 at/cm² level (higher concentration tested), the discrepancies are lower and close to being in agreement in regards with the respective uncertainties. There are several possible reasons for these deviations. First of all, the analysed area or the size of the excited area of the sample is drastically different for all methodologies. While this area is in the order of several mm x 150 µm for the PTB TXRF analysis, it is about 4 cm² for the LETI TXRF analysis and the nearly the full surface of the 100 mm Si wafer for the VPD-ICPMS. As a result, lateral inhomogeneities of the spin coated concentration of the contaminants could be a reason for these deviations. If the overall contamination level is low, these inhomogeneities are likely to be significant on the local scale. The PTB TXRF results where only performed in the center of the wafer for most samples. Secondly, the wafer handling at PTB is not fully clean room conformable as we need to handle the wafers manually. They were mounted in a local clean room atmosphere onto the sample holder, transferred to the experimental setup in a sealed box and then mounted in the chamber. Even though we do not expect additional surface contaminations of Al, Ni and Mo due to this handling, it could result in other contaminations that negatively influence the quantification.

For a validation of the contamination issues, additional TXRF experiments were performed at Leti in clean room conditions on the wafers after their return from PTB. These experiments indeed show a cross-contamination induced by shipping and PTB handling and environment conditions. Indeed contaminated wafers as well as the Reference clean Si wafer added as witness sample clearly highlight a significant additional metallic contamination occurred in mainly Fe, Ca, Cr, Mn (> E12 at/cm²), Mn, Cu and even Ni (E11 at/cm² range). Also, a full surface analysis by VPD ICPMS of the Ref clean Si-wafer has showed an addition of Al, Ni and Mo contamination (resp. 8.1 E11 at/cm², 0.2 E10 at/cm² and 9.7 at/cm²). Such cross contamination is quite expected in no clean room or in not adapted handling conditions. As a result, shipping & handling conditions of wafers samples led to significant additional contaminations likely as particles, these ones being especially non negligible at local scale and/or for wafers at lower contamination doses and can explain some observed discrepancies.



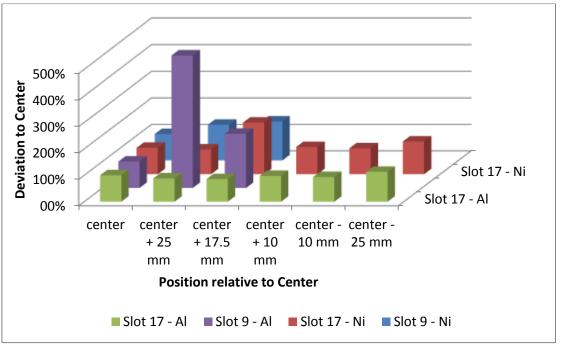


Figure 25. Relative deviation of quantified mass depositions for Al and Ni at different positions with respect to the center of the corresponding wafer. The value for Slot 9 – Al at +25 mm is not within the present y-scale (+5810 %).

Due to these large deviations, we have performed additional experiments using the PTB TXRF methodology in order to investigate the lateral homogeneity of the spin coated samples. Therefore, we have performed quantification also on different positions with respect to the center across the wafer surface. The corresponding results for two of the available wafers and two of the prepared contaminants are shown in Figure 25. Here, a significant inhomogeneity of the samples could be revealed across larger areas of the surface. Please note the large deviation for the value for Al at E12 at/cm² (Slot 9) at +25 mm which is not even within the presented y-scale (+5810 %). Additional local (particles) contamination could contribute to such a huge discrepancy. To also cross check the short scale homogeneity, we have performed a line scan on sample E14 at/cm² (Slot 17) in the vicinity of the center of the wafer. The corresponding deviation of the Ni mass deposition with respect to the center position is shown in Figure 26. Also here, a relatively large inhomogeneity can be revealed, this one being likely mainly due to the spin coat/dry contamination process itself.

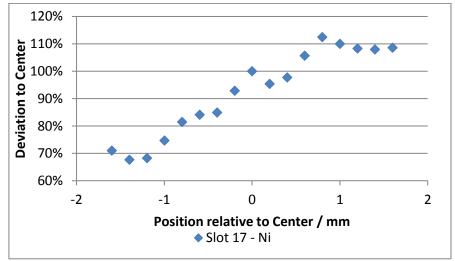


Figure 26. Lateral homogeneity of the Ni mass deposition on sample Slot 17 in close proximity to the center position of the wafer.



In summary, thickness uniformity and surface quality of wafers/dies thinning (in the presence of circuits) have been assessed together with the surface contamination using traceable metrology and techniques leading to full achievement of this objective.

5 Impact

A brief summary of the dissemination activities undertaken

The Consortium have organised several workshops and events for dissemination: stakeholder workshops were held at IMEC in December 2016, at the EMRS Spring Conference in May 2017 within the ALTECH symposium, at CEA Leti in September 2017 and at the semi European 3D Summit in January 2018

Impact on relevant standards

This project will have a direct impact on the semiconductor industry by addressing the key metrology challenges and technologies required for 3D heterogeneous integration. Information on the progress and results of the project will be disseminated to International and European standard bodies and committees in this field and recommendations will be made when appropriate. This project has dedicated an important part of the work to produce specific technical standards documents, Good Practice Guides and Guides for Conformity assessment targeted at the stakeholder community and particularly International and European standards bodies and committees (ISO/IEC Committees). The project consortium is represented in the technical product specifications and verification. The high speed large range metrological AFM has been evaluated as being a good candidate for measuring 3D areal measurement parameters and a novel physical material has been developed for instrument transfer function and topography fidelity of 3D areal measurement and two Good practice guides have been produced and made publically available from the project website.

Impact on industrial and other user communities

This project will provide a clear industrial exploitation path towards further functionality for TSV based 3D-SICs devices, while lowering manufacturing costs and time to market. Focusing on industrial needs and having participants who are an integral part of the semiconductor industry value chain (R&D labs, Integrated Device and end-equipment Manufacturers) will ensure an effective transfer of the results of this project into industry, reinforced by work on the standardisation of key technologies, design parameters and processes.

The European semiconductor supply chain is entirely engaged in this project, either as partners – Fogale, CEA, FhG and IMEC - or as collaborators providing state of the art samples and steering assistance. Indeed, to ensure a direct industrial relevance, the consortium has created a stakeholder committee of 7 members. Experts from both industry and academy have joined, among them market leaders such as Keysight Technologies, Thales, IQEP and KLA-Tencor.

As examples of uptake from project outputs, the lock-in thermography set-up has been used to identify hot spots in new electronic devices in collaboration with an industrial partner, and TSV and solder bump array samples have been provided to Bruker Nano GmbH for comparison experiments using a laboratory setup. Other examples of uptake and exploitation are linked with the delivering of a circular chirp standard to four different companies in the field for characterising the metrology properties of optical areal surface metrology tools. Also, KLA-Tencor has expressed interest to check potential of the use of GHz-SAM as an in-line tool.

Impact on the metrological and scientific communities

This project will have an immediate impact by providing traceable facilities for the calibration standards and measurements of thermal and electrical material characterisation, defects inspection for high-aspect ratio TSV and wafer/chip bonding and thinning processes to existing European companies through its trade association – European Semiconductor Industry Association (ESIA). The development of the metrological tools and procedures will help the transfer of metrology solutions between R&D laboratories and fabrication centres, thereby increasing the extent of cooperation, and adding metrology to established techniques. Moreover, success in this area will support the further development of nano-engineering and other advanced techniques, creating new opportunities to improve the semiconductor devices used for widespread applications in the Key Enabling Technologies (nanoelectronics, photonics, biotechnologies, energy).

PTB is now offering the following nanodimensional calibration services: step height standards, depth-setting standards, 1D lateral standards, 2D lateral standards, 3D Nano standards and reference areal surface metrology. CMI have introduced a new calibration service based on the techniques developed in the project,



which provides local thermal measurement using a developed SThM system. CMI is now offering such service via direct communication to partners from the semiconductor industry and conferences like Therminics.

Longer-term economic, social and environmental impacts

Having many semi-conductor supply chain partners in his projects emphasises the critical need for metrological tools to accelerate the introduction of 3D-SICs. While the technologies provided by this project are beneficial for the worldwide adoption of TSV based 3D heterogeneous integration, the European development of the metrology process will allow Europe to play a more important role in the supply chain for future information systems built using highly dense electronics, and will create an enduring competitive advantage for Europe.

The project will also support the Digital Agenda for Europe within the Initiative 2020 Action 129: Pooling of European public and private resources for the micro- and nano-electronics behind a common industrial strategy and the Key Enabling Technologies Initiative (KET) established in 2011. This project is our contribution to the European industrial strategy for micro/nano electronics published on 14 February 2014 with the ambitious goal to get around 20 % of semiconductor manufacturing back to Europe by 2020.

6 List of publications

- "Investigating stress measurement capabilities of GHz scanning acoustic microscopy for 3D failure analysis", .A. Khaled, S. Brand, M. Kogel, T. Appenroth, I. De Wolf, Microelectronics Reliability, http://dx.doi.org/10.1016/j.microrel.2016.07.061
- "Development and characterization of sub-monolayer coatings as novel calibration samples for X-ray spectroscopy", P. Hönicke, M. Krämer, L. Lühl, K. Andrianov, B. Beckhoff, R. Dietsch, T. Holz, B. Kanngiesser, D. Weißbach, T. Wilhein, Spectrochimica Acta B, 10.1016/j.sab.2018.04.001
- "Accurate experimental determination of Gallium K- and L3-shell XRF fundamental parameters", R. Unterumsberger, P. Hönicke, J. Colaux, C. Jeynes, M. Wansleben, M. Müller, B. Beckhoff, J. Anal. At. Spectrom., 10.1039/C8JA00046H
- "Fast and accurate: high-speed metrological large-range AFM for surface and nanometrology", G. Dai, L. Koenders, J. Fluegge, M. Hemmleb, Measurement Science and Technology, <u>https://doi.org/10.1088/1361-6501/aaaf8a</u>