Publishable Summary for 14IND07 3D Stack
Metrology for manufacturing 3D stacked integrated circuits

Overview

In February 2014, the European Electronic Leaders Group, representing the main companies in the sector, identified 3D integration of heterogeneous semiconductor technologies as the key opportunity for growth in Europe. 3D integration technology uses copper Through Silicon Vias (TSV) to electrically connect a stack of chips-bonded semiconductor wafers and dies to produce 3D stacked integrated circuits (3D-SICs) with an optimum combination of cost, functionality, performance and power consumption. This project has brought solutions to overcome the lack of traceable measurement tools and methods for reliability assessment of TSV-based 3D heterogeneous integration, by developing reference materials and calibrated standards and measurements, certified and tested, for the introduction of these 3D-SICs and enabling the progress of the electronics industry in Europe.

Need

While this technology is already used in imagers, memories and MEMS, its extension into new areas required a much larger density of higher aspect-ratio, smaller TSVs. This has created new metrological issues related to the dimensional and electrical characterisation of these TSVs and to the characterisation of heat caused by the higher current density in those structures.

Another aspect of this technological vision was that each function of the 3D stack samples (i.e. memory, sensor, biochip) can be manufactured independently at the right node (the node is the number representing the lowest size of the chip features) and in an optimised production line. 3D integration allowed them to be combined into a single compact system, with logic devices, memories, imagers and MEMS structures from different wafers (from various foundries) using different manufacturing processes. However, this introduced new traceability requirements in the metrology for 3D integration, as for instance for TSVs with a high aspect ratio which requires complete profile shape information. In fact, for this kind of TSV, any deviation from the targeted profile - such as undercut or bottom distortions or even high roughness or the non-conformity of the isolation of the barrier and seed layer was an important issue. An increase in the resistivity can be observed in TSVs having reduced dimensions and copper (Cu) having a small grain size and this needed accurate electrical nanoscale measurements.

Objectives

This project focuses on developing the traceable measurement capabilities for structural and chemical defects inspection in high aspect ratio through silicon vias (HAR TSV) and wafer/chip bonding and thinning. The JRP will also develop new accurate measurement techniques for thermal and electrical materials characterisation at the nanoscale of the TSVs with the following objectives;

1. To develop reliable 3D characterisation techniques, protocols and standards to accurately measure (at micron and submicron resolution) dimensional and structural properties of high aspect ratio (HAR>10) TSV interconnects before and after Cu filling: sidewall roughness, via shape, seed- and barrier-layer thickness, sidewall layer conformity, void detection and characterisation, grain size and grain boundary character distribution of the copper grains, crystalline structure, dislocations, stress around the TSV. In addition, for 3D-SICs with high density TSV interconnects, it is important to consider non-destructive wafer measurements as well as statistical data collection to enable the implementation of the measurement techniques in a production environment.

2. To develop methods to accurately measure the electrical and thermal transport properties of nanostructured copper TSV interconnects in order to establish traceable measurements of electrical conductivity and temperature change in copper as a function of the current density. Modelling of thermal transport in those structures will help to identify the various thermal scattering mechanisms in nanostructured copper grains.
3. To develop metrology tools, protocols and standards for high lateral and z resolution (sub microns for x-y, nm for z) non-destructive wafer to wafer alignment control before and after bonding as well as the characterisation of the bonding quality of wafers and dies: parameters at die level such as curvature, surface roughness and flatness which might need to be coupled with wafer level information; wafer/die contamination before bonding; wafer/die interface defectivity and adhesion after bonding; local stress and thermal dissipation at the interface of bonding wafers and dies will also be considered.
4. To provide traceable metrology for thickness uniformity control and for the surface quality of wafers/dies thinning (in the presence of circuits) and measurement techniques related to stress relaxation, crystalline defects and surface contamination.
5. To engage with the semiconductor industry and others to facilitate the take up of the technology and measurement infrastructure developed by the project, to support the development of new, innovative products utilising 3D-stacked ICs, thereby enhancing the competitiveness of EU industry.

Progress beyond the state of the art

The evolution of the More than Moore approach (which adds digital and non-digital functional diversification to the miniaturisation of the digital functions) has introduced 3D objects at the micron scale to TSV and 3D heterogeneous integration. 3D characterisation, metrology, and inspection with micrometric to nanometric resolution and capabilities of large-field analysis to inspect and measure groups of vias were required as well as controlling wafer/chip thinning and bonding processes.

Prior to the start of this project, measurement techniques were suffering from a lack of traceability, accuracy and quantification. This project has focused on establishing traceability of existing instruments (optical based methods) by developing new standards and reducing uncertainty through new measurement protocols and methodologies. It has proposed to develop new instrumentation (Scanning Probe Microscopy, Scanning Acoustic Microscopy and Synchrotron based methods) to characterise the TSVs before and after filling as well as characterisation of the bonding and thinning quality of wafers and dies.

Results

1. *3D characterisation techniques, protocols and standards to accurately measure dimensional and structural properties of high aspect ratio TSV interconnects*

The 3D Stack project has developed techniques and methodologies to enable the traceable and accurate characterisation of the dimensional and structural properties of HAR TSVs devices before and after Cu filling. Reference materials, calibrated standards and measurements have been made available to overcome the current lack of traceable measurement tools and methods for reliability assessment of TSV based 3D integration technology and to extend this technology to the large-scale manufacturing of mainstream consumer applications and emerging 3D-SIC nanoelectronic devices.

In line with the sample tracking document that has been established for the definition of the characteristics of filled and non-filled Cu TSV samples and shared among the partners, samples with Cu filled TSVs and other structures using TSVs, cross-sectioned and polished samples have been distributed to the partners. A novel 3D-AFM with different measurement strategies for non-destructive measurements of dimensional properties of TSVs has been developed. Traceable scanning electron microscopy (SEM) and atomic force microscopy (AFM) measurements have been performed for the dimensional and structure characterisation on cross-sectioned TSVs. Various optical techniques for large profilometry (confocal, white light interferometry, IR interferometry, optical microscopy…) were applied and compared to AFM, to measure dimensional properties of TSVs. White light microscopy and AFM measurements were performed to study Cu-pumping (irreversible extrusion of copper from Cu-filled TSVs exposed to high temperatures during back-end of line (BEOL) processing) in TSVs with various dimensions. Different characterisations and measurements have been carried out, like non-destructive measurement of dimensional properties of TSVs using a novel 3D-AFM, dimensional and structure characterisation on cross-sectioned TSVs using X-ray and µX-ray fluorescence

(XRF) mappings in order to reveal voids and contaminants and work on the reduction of the uncertainty budget of the reference-free XRF quantification has been carried out by performing both experimental determinations and validations of the relevant atomic fundamental parameters. Grain size, orientation and grain boundary properties were characterised using light microscopy and SEM. Work was also carried out to assess the SMM technique on its capability to detect voids and sidewall delamination and it has been proven to be an inadequate approach due to limited penetration depths of the high frequency microwaves and that significantly lower frequencies in the kHz-range should be used. Experiments and tests performed on the use of gigahertz scanning acoustic microscopy (GHz-SAM) indicated that the technique has very promising features, but that it is not ready for implementation in the fab (foundry) and for standardisation. The detection of TSV voids by GHz-SAM was not proven with present instrumentation and it has been shown that it needs to be optimised for such a measurement and be more stable in terms of distance between the transducer and the sample during the scan. Dimensional structures of high aspect ratio TSVs were also measured by preparation of cross-sectioning of silicon wafer and ion milling techniques for polishing. Measurement on SEM pictures revealed dimensional data as TSV diameter in different depth, total TSV depth as well as barrier thickness. Microstructural analysis was also carried out with good contrast and high resolution in the range of 100 nm using ion channelling in the FIB tool. Samples were prepared by mechanical cross-sectioning, polishing and ion milling.

Even if some techniques have had their efficacy not fully demonstrated like GHz-SAM and SMM, the objective can be considered to be achieved in terms of the different parameters that had to be characterised for all techniques combined.

2. *Methods to accurately measure the electrical and thermal transport properties of nanostructured copper TSV interconnects*

This project has also focused on the development of methods to accurately measure electrical and thermal transport properties of nanostructured copper TSV interconnects in order to establish traceable local measurements of electrical conductivity and temperature change in copper as a function of the current density.

A lock-in thermography set-up has been developed to accurately measure the temperature change in electronic devices and it can be used for calibrating scanning thermal microscopy (SThM) measurements. Instrumentation for measuring thermal transport for thin-films for various temperatures has been designed and built, and full uncertainty budget has been reported for the power dissipated and the localised temperature. Other characterisation and measurement systems have been improved, with first measurements with scanning microwave microscopy (SMM) on angle polished samples allowing analysis based on varying either TSV size or microwave frequency and using two design independent SMM systems by two project partners to increase confidence. Determining a single TSV's resistivity with the SMM was unsuccessful due to limited sensitivity because of the too high electrical conductivity of copper and the too small dimensions involved. Only qualitative information about the different electrical properties between the copper and silicon surfaces has been extracted for these samples using either SMM or C-AFM. The copper resistivity measurement using both systems has been difficult, because of technical limitations of each technique. Also, a system to measure resistivity at the micro scale has been upgraded in terms of positioning precision, probe resolution and electrical parameter sensitivity and resistivity measurement of copper filled TSVs was carried out.

This objective was not fully achieved considering the limit of the implemented electrical techniques to characterise a high electrical conductivity such as that for copper in microscale dimensions.

3. *Metrology tools, protocols and standards for non-destructive wafer to wafer alignment control and characterisation of the bonding quality of wafers and dies*

There are several technological challenges in bonding and thinning process control that are unique for 3D integration technology and that could be solved by the work undertaken in this project. This has led to the development of high lateral and z resolution wafer to wafer alignment control before and after bonding as well as the characterisation of the bonding quality of wafers and dies. Most of the measurement techniques, procedures and methodologies developed have been validated including establishing uncertainty budgets so that high accuracy is achieved and traceability ensured.

Several samples have been prepared and distributed to the partners, based on a shared list that has been established from the inputs of all the participants, defining the characteristics of samples, including arrays of interconnect structures, thinned wafers, bonded wafers/dies with wafers, TSV interconnects, wafer bumps and bump arrays, and 3D assemblies. Experiments with laser scanning IR microscopy have been carried out to study its applicability for thickness measurements and the assessment of the X-Y resolution. Thickness measurements using IR laser scanning was assessed on dedicated samples which were prepared by local thinning and have shown the limitations of such a technique because the light used is monochromatic and for this reason any change in thickness or tilt of the sample will give rise to interference fringes which might affect the measurement results.

A high speed large range metrological AFM has been developed that allows scan speeds up to 1 mm/s and a measurement volume of 25 mm x 25 mm x 5 mm. Measurement experiments on a cleaved post chemical-mechanical planarization (CMP) wafer were performed, showing promising performance.

White Light Interferometer (WLI) measurements correlated with SMM measurements gave precise results on topography of the base wafer. The apex of the bumps was also in many cases resolved and extensive software analysis with homemade software was performed to be able to extract statistic parameters of the bumps.

SEM and light microscopy have been used together in order to control stacking quality and total thickness variation (TTV), bow and warpage measurements have been performed on 300 mm wafer.

Post bonding overlay measurement using various optical techniques was assessed and several issues were raised like the choice of size, pattern shape and material, the good conditions for alignment check and the use of wafer backside illumination versus camera position for higher contrast.

All these results will give more confidence in the assessment of key dimensional parameters like curvature, roughness, flatness and alignment which are necessary for the control of the wafer/dies thinning and bonding processes, crucial for 3D heterogeneous integration technology.

This objective was achieved considering the several metrology tools that have been implemented for wafer to wafer alignment control before and after bonding.

4. Traceable metrology for thickness uniformity control and for the surface quality of wafer/die thinning

This project has developed measurement tools and methodologies to characterise the surface and interface quality, which is related with thickness uniformity, of bonded/thinned wafers and dies in terms of contamination, interface defectivity and adhesion, stress relaxation and thermal dissipation.

Experiments on Cu thin foils have been carried out and the K-shell fluorescence yield as an atomic fundamental parameter as well as the respective transition probabilities have been determined with well-known uncertainties. This material can be used for more reliable calibration purposes. In addition, oxidation studies on Co, Cu and Ni metal layers were performed. Also, sensitivity of Raman spectroscopy to surface damage and thickness variations due to the thinning process of wafers or even sensitivity of micro-Raman spectroscopy to the presence of mechanical stress in local areas of a wafer have been demonstrated.

This objective was achieved with the assessment of thickness uniformity and surface quality of wafers/dies thinning using traceable metrology and techniques.

Impact

A brief summary of the dissemination activities undertaken

The Consortium have organised several workshops and events for dissemination: stakeholder workshops were held at IMEC in December 2016, at the EMRS Spring Conference in May 2017 within the ALTECH symposium, at CEA Leti in September 2017 and at the semi European 3D Summit in January 2018

Impact on relevant standards

This project will have a direct impact on the semiconductor industry by addressing the key metrology challenges and technologies required for 3D heterogeneous integration. Information on the progress and results of the project will be disseminated to International and European standard bodies and committees in this field and recommendations will be made when appropriate. This project has dedicated an important part of the work to produce specific technical standards documents, Good Practice Guides and Guides for

Conformity assessment targeted at the stakeholder community and particularly International and European standards bodies and committees (ISO/IEC Committees). The project consortium is represented in the technical committees ISO TC201 for surface chemical analysis and ISO TC213 for dimensional and geometrical product specifications and verification. The high speed large range metrological AFM has been evaluated as being a good candidate for measuring 3D areal measurement parameters and a novel physical material has been developed for instrument transfer function and topography fidelity of 3D areal measurement tools characterisation and was to be presented to ISO/TC 213/WG 16. Two Guides to Conformity assessment and two Good practice guides have been produced and made publically available from the project website.

Impact on industrial and other user communities

This project will provide a clear industrial exploitation path towards further functionality for TSV based 3D-SICs devices, while lowering manufacturing costs and time to market. Focusing on industrial needs and having participants who are an integral part of the semiconductor industry value chain (R&D labs, Integrated Device and end-equipment Manufacturers) will ensure an effective transfer of the results of this project into industry, reinforced by work on the standardisation of key technologies, design parameters and processes.

The European semiconductor supply chain is entirely engaged in this project, either as partners – Fogale, CEA, FhG and IMEC - or as collaborators providing state of the art samples and steering assistance. Indeed, to ensure a direct industrial relevance, the consortium has created a stakeholder committee of 7 members. Experts from both industry and academy have joined, among them market leaders such as Keysight Technologies, Thales, IQEP and KLA-Tencor.

As examples of uptake from project outputs, the lock-in thermography set-up has been used to identify hot spots in new electronic devices in collaboration with an industrial partner, and TSV and solder bump array samples have been provided to Bruker Nano GmbH for comparison experiments using a laboratory setup. Other examples of uptake and exploitation are linked with the delivering of a circular chirp standard to four different companies in the field for characterising the metrology properties of optical areal surface metrology tools. Also, KLA-Tencor has expressed interest to check potential of the use of GHz-SAM as an in-line tool.

Impact on the metrological and scientific communities

This project will have an immediate impact by providing traceable facilities for the calibration standards and measurements of thermal and electrical material characterisation, defects inspection for high-aspect ratio TSV and wafer/chip bonding and thinning processes to existing European companies through its trade association – European Semiconductor Industry Association (ESIA). The development of the metrological tools and procedures will help the transfer of metrology solutions between R&D laboratories and fabrication centres, thereby increasing the extent of cooperation, and adding metrology to established techniques. Moreover, success in this area will support the further development of nano-engineering and other advanced techniques, creating new opportunities to improve the semiconductor devices used for widespread applications in the Key Enabling Technologies (nanoelectronics, photonics, biotechnologies, energy).

PTB is now offering the following nanodimensional calibration services: step height standards, depth-setting standards, 1D lateral standards, 2D lateral standards, 3D Nano standards and reference areal surface metrology. CMI have introduced a new calibration service based on the techniques developed in the project, which provides local thermal measurement using a developed SThM system. CMI is now offering such service via direct communication to partners from the semiconductor industry and conferences like Therminics.

Longer-term economic, social and environmental impacts

Having many semi-conductor supply chain partners in his projects emphasises the critical need for metrological tools to accelerate the introduction of 3D-SICs. While the technologies provided by this project are beneficial for the worldwide adoption of TSV based 3D heterogeneous integration, the European development of the metrology process will allow Europe to play a more important role in the supply chain for future information systems built using highly dense electronics, and will create an enduring competitive advantage for Europe.

The project will also support the Digital Agenda for Europe within the Initiative 2020 Action 129: Pooling of European public and private resources for the micro- and nano-electronics behind a common industrial strategy and the Key Enabling Technologies Initiative (KET) established in 2011. This project is our contribution to the European industrial strategy for micro/nano electronics published on 14 February 2014 with the ambitious goal to get around 20 % of semiconductor manufacturing back to Europe by 2020.

List of Publications

1. "Investigating stress measurement capabilities of GHz scanning acoustic microscopy for 3D failure analysis", .A. Khaled, S. Brand, M. Kogel, T. Appenroth, I. De Wolf, Microelectronics Reliability, http://dx.doi.org/10.1016/j.microrel.2016.07.061
2. "Development and characterization of sub-monolayer coatings as novel calibration samples for X-ray spectroscopy", P. Hönicke, M. Krämer, L. Lühl, K. Andrianov, B. Beckhoff, R. Dietsch, T. Holz, B. Kanngiesser, D. Weißbach, T. Wilhein, Spectrochimica Acta B, 10.1016/j.sab.2018.04.001
3. "Accurate experimental determination of Gallium K- and L3-shell XRF fundamental parameters", R. Unterumsberger , P. Hönicke, J. Colaux , C. Jeynes, M. Wansleben, M. Müller, B. Beckhoff, J. Anal. At. Spectrom., 10.1039/C8JA00046H
4. "Fast and accurate: high-speed metrological large-range AFM for surface and nanometrology", G. Dai, L. Koenders, J. Fluegge, M. Hemmleb, Measurement Science and Technology, https://doi.org/10.1088/1361-6501/aaaf8a

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Internal Funded Partners: 1 LNE, France 2 CMI, Czech Republic 3 NPL, UK 4 PTB, Germany	External Funded Partners: 5 CEA, France 6 FhG, Germany 7 IMEC, Belgium	Unfunded Partners: 8 FOGALE, France 9 METAS, Switzerland